COVER SHEET FOR GRANT PROPOSALS

State Board of Education

SBOE PROPOSAL NUMBER: (to be assigned by SBOE)	AMOUNT REQUESTED: **50,000.00 USD**

TITLE OF PROPOSED PROJECT:
SSLAR Imaging System Development for High-speed, High-resolution Surveillance Camera Markets

SPECIFIC PROJECT FOCUS:
Development of commercial grade surveillance camera prototype with a high resolution, low-power consumption and high-frame rate image sensor

PROJECT START DATE: **09/01/2011**	PROJECT END DATE: **08/31/2012**
NAME OF INSTITUTION: **University of Idaho**	DEPARTMENT: **Electrical and Computer Engineering**

ADDRESS: **Department of Electrical and Computer Engineering, P.O. Box 441023, Moscow, ID, 83844-1023**

	E-MAIL ADDRESS:	PI PHONE NUMBER:
	suatay@uidaho.edu	**208-885-2783**

	NAME:	TITLE:	SIGNATURE:
PROJECT DIRECTOR	**Suat Utku, Ay**	**Assistant Professor**	
CO-PRINCIPAL INVESTIGATOR			
CO-PRINCIPAL INVESTIGATOR			
CO-PRINCIPAL INVESTIGATOR			

	NAME:	SIGNATURE:
Authorized Organizational Representative	**Polly Knutson**	
	Polly J Knutson, Director Office of Sponsored Programs University of Idaho SK	by 5/26/11

SUMMARY PROPOSAL BUDGET

Name of Institution: **University of Idaho**

Name of Project Director: **Suat Utku Ay**

A. FACULTY AND STAFF

Name/ Title	Rate of Pay	No. of Months CAL	ACA	SUM	Dollar Amount Requested
Suat Utku Ay / Assistant Professor	**62.28**			**0.75**	**7,500.00**
% OF TOTAL BUDGET: **15%**			**SUBTOTAL:**		**7,500.00**

B. VISITING PROFESSORS

Name/ Title	Rate of Pay	No. of Months CAL	ACA	SUM	Dollar Amount Requested
% OF TOTAL BUDGET:			**SUBTOTAL:**		**0.00**

C. POST DOCTORAL ASSOCIATES / OTHER PROFESSIONALS

Name/ Title	Rate of Pay	No. of Months CAL	ACA	SUM	Dollar Amount Requested
% OF TOTAL BUDGET:			**SUBTOTAL:**		**0.00**

D. GRADUATE / UNDERGRADUATE STUDENTS

Name/ Title	Rate of Pay	No. of Months CAL	ACA	SUM	Dollar Amount Requested
TBD/Research Assistant (Graduate Student, 20hr/week)	**16.00**		**4.875**	**0.75**	**7,200.00**
% OF TOTAL BUDGET: **14.4%**			**SUBTOTAL:**		**7,200.00**

E. FRINGE BENEFITS

Rate of Pay (%)	Salary Base	Dollar Amount Requested
PI:24% (SUM)	**97,157.00 (ACA)**	**1,800.00**
RA: 1% (ACA), 9%(SUM)	**12,480.00 (ACA)**	**200.00**
	SUBTOTAL:	**2,000.00**

F. EQUIPMENT: (List each item with a cost in excess of $1000.00.)

Item/Description	Dollar Amount Requested
SUBTOTAL:	**0.00**

G. TRAVEL: NONE

Dates of Travel (from/to)	No. of Persons	Total Days	Transportation	Lodging	Per Diem	Dollar Amount Requested
						0.00
						0.00
						0.00
					SUBTOTAL:	**0.00**

H. Participant Support Costs:

	Dollar Amount Requested
1. Stipends	**0.00**
2. Travel (other than listed in section G)	**0.00**
3. Subsistence	**0.00**
4. Other	**0.00**
SUBTOTAL:	**0.00**

I. Other Direct Costs:	Dollar Amount Requested
1. Materials and Supplies	27,800.00
2. Publication Costs/Page Charges	
3. Consultant Services (Include Travel Expenses)	
4. Computer Services	
5. Subcontracts	
6. Other (specify nature & breakdown if over $1000) **Cadence IC design ($5,000) software and PCB Design software ($500)**	5,500.00
SUBTOTAL:	33,300.00
J. Total Costs: (Add subtotals, sections A through I) **TOTAL:**	50,000.00
K. Amount Requested: **TOTAL:**	50,000.00
Project Director's Signature: **Suat Utku Ay**	Date: 05/26/2011

INSTITUTIONAL AND OTHER SECTOR SUPPORT

(add additional pages as necessary)

A. INSTITUTIONAL / OTHER SECTOR DOLLARS

Source / Description	Amount

B. FACULTY / STAFF POSITIONS

Description

C. CAPITAL EQUIPMENT

Description

D. FACILITIES & INSTRUMENTATION

Description

SSLAR IMAGING SYSTEM DEVELOPMENT FOR HIGH-SPEED, HIGH-RESOLUTION SURVEILANCE CAMERA MARKET

1. Faculty member directing project: Suat Utku Ay

2. Name of Idaho public institution: University of Idaho

3. Objective and amount requested: High-resolution, high-speed digital cameras are currently the fastest growing segment of the surveillance market worldwide. According to Frost & Sullivan (F&S), the worldwide digital camera market is expected to grow by more than 20% per year from $2.7 billion USD in 2010 to $4.8 billion by 2016. Most major image sensor companies are developing new digital video camera product lines to capture a portion of this market. They typically do this by expanding their current product lines that were originally optimized for the high-volume, low video rate (15-30 frames/s) consumer markets, such as cell phones and digital still cameras. The main dilemma companies are facing is to balance return of investment, design risk, and meeting the surveillance market demand for 1) high resolution (720p HD or better), 2) low-power consumption (<250mW), and 3) high-frame rate (>120frames/s) imaging. For a typical image sensor company, addressing resolution is not a problem. However, using current circuit Intellectual Properties (IP) for the new designs does not address the low-power and high speed operation requirements for advanced digital cameras surveillance applications. This forces companies to develop a new product line investing heavily on new design techniques, technologies, and circuit IP which increase risk and effect profitability. Seeing an opportunity, the PI (Suat Ay) has developed a patent protected algorithm and circuit IP that addresses the need for speed and low-power consumption, all without sacrificing image quality. Called the single-slope look-ahead ramp (SSLAR) analog-to-digital converter (ADC) technology, it is designed to meet this market demand for high-speed, high-resolution, and low-power camera

systems. SSLAR ADC technology scales linearly (in terms of bit-resolution and power consumption) as opposed to the current ADC technologies used in CMOS image sensor thereby reducing design risk. PI has already designed and fabricated integrated circuits (IC) that prove the effectiveness of the SSLAR technology under laboratory conditions.

We are requesting $50,000 of incubation funds to develop an HD 720 format CMOS image sensor and to build a for-profit corporation to commercialize the developed image sensor and related technologies. Three specific tasks identified to achieve the goals are: 1. Design and fabrication of a commercial grade HD-720 format SSLAR imager sensor integrated circuit (IC). 2. Integration of the designed SSLAR imager IC into a demonstration and development system with commercial grade software and hardware. 3. Develop a business plan for successful commercialization of the SSLAR technology and fund a for-profit corporation spinning off SSLAR IP from UI.

SSLAR technology has already been demonstrated in laboratory environments with smaller array formats (136x136) image sensors with technology readiness level (TRL) of 4. Through this funding, we will achieve TRL level of 7, bringing the technology close for commercialization.

4. Resource commitments reflect priority: Resource allocations of project personal and funds are shown on Table 2. Dr. Ay already has a laboratory with necessary equipment and tools for image sensor design, characterization and testing that will be used to support this project. This proposed project is aligned with the priority of the University's Office of Technology Transfer (OTT) to promote the timely transfer of commercially viable technology to the private sector.

5. Impact to economy of Idaho: Peter Sutherland of Peter G. Sutherland & Associates, LLC and President of the Inland TechStart Fund, LLC, a seed capital investment fund, has identified the SSLAR camera chip technology and other high speed ADC technology at UI as the basis for a

commercialization opportunity. Sutherland will personally mentor a startup company at the UI Microelectronic R&D facility incubator to further develop the technology in conjunction with the UI Office of Technology Transfer and the inventor (Suat Ay) and license the SSLAR camera chip technology in order to build a company that can provide both SSLAR camera chip sets and digital video cameras for the video surveillance markets. Within a two-year period Mr. Sutherland expects to employ 10-20 people in the Post Falls/Coeur d'Alene area and have revenues in the range of $1M-$5M. The company is expected to grow rapidly after that time and has the opportunity to become a significant supplier of digital cameras to the video surveillance and other high resolution camera markets.

The integration of the patented SSLAR ADC with CMOS image sensors allows for a new generation of digital video cameras to be developed for multiple applications such as video surveillance, perimeter security, and high resolution photography. The inherent capability of the SSLAR ADC to increase the conversion speed of images from the CMOS image sensors with minimal loss of image quality (less than 1%) allows for a digital video camera to operate in multiple modes while minimizing the need for transmission and storage of unneeded data. This solution will save significant bandwidth in transmission and storage space yet give full motion high resolution video when needed.

Most analog video surveillance cameras today are programmed to take snapshots every couple of seconds so that the video files are not too large to store or transmit to another location for viewing or storage. New IP digital video camera designs are overtaking the analog cameras for most of these surveillance applications that use data compression techniques (i.e. H.264 standards) to minimize the transmission bandwidth and storage capacity. Many of these new digital cameras are in fixed locations with fixed lenses but require reasonably high speed transmission such as fiber, coax or Ethernet. These new IP digital cameras operate at a fixed

speed all of the time with storage requirements for video measured in Terabits instead of Gigabits.

While our initial SSLAR chip development will focus on a 1 Megapixel digital video (1280 X 720 array) camera that will be used for fixed surveillance applications, where events only occur occasionally and the event needs higher speed and resolution when it occurs (i.e. intrusion), the SSLAR technology can be used in a much broader set of surveillance applications with higher resolution (i.e. 2-8 Megapixels). This initial SSLAR camera chipset will use less power and provide much more efficient use of transmission bandwidth and storage capacity for video files. It will be physically very small and electronically sensor driven for event recording even in low level light conditions. The initial SSLAR camera can be wired to the internet via standard telephone two wire systems, Ethernet, coax cable or via wireless transmission.

A recent In-Stat report, *Video Surveillance: Analog and IP cameras, DVRs, NVRs, Analytics, Semiconductor and Technology* forecast the video surveillance market will approach $15 Billion by 2014 and is growing at a robust 7%-9% per year. In-Stat forecasts that IP cameras will overtake analog cameras this year with higher resolution (H.264 or better). While the camera is only a portion of a video surveillance system it is the most important part since it drives the data compression, transmission and data storage equipment requirements. F&S forecasts in their recent *Global Video Surveillance Market* report that analog and IP and digital video camera revenue will grow from $2.9M to $4.7M by 2016 and that IP and digital video cameras will represent more than 50% of the market or $2.8B by 2016. This is more than a 20% compound annual growth rate for IP digital video cameras for surveillance applications alone. The majority of these digital video cameras will be 1 to 5 Megapixels resolution and be priced from $160 to $700 by 2014.

While there are a number of enhancements of the CCD and CMOS imaging technology to increase resolution and improve low light level performance and the image and storage compression processors are becoming faster there has been relatively little improvement in the analog to digital converters in the cameras. We believe the opportunity exists for a new generation of IP digital video camera chip sets that can integrate the CMOS imaging directly with the SSLAR ADC with various resolution and frame rates that can be electronically scaled for an event recording without increasing power consumption by the camera. This frame rate adjustment ability, coupled with the lower static data transmission requirements and lower storage capacity requirements, will make a dynamic video camera for the surveillance market.

The size of the market opportunity for a commercialization of the SSLAR camera chip technology depends on whether we team with video surveillance camera companies and sell them chip sets with software algorithms or we build complete SSLAR digital video cameras for surveillance applications described above. In either case we believe the current available market in video surveillance applications that can be served is in the $300M - $500M size and is only limited by the adoption rate of the SSLAR camera chip technology and the ability to fund a company to manufacture and distribute the products. The served available market for the 1-5 Megapixel SSLAR digital cameras will grow to at least $1B by 2016 according our analysis.

6. Specific project plan and detailed use of funds: Project is organized into three tasks as shown on the Table 1. Funds will be used to achieve first two tasks while commercialization partner will bear the cost of the third task committing appropriate resources.

First task is related to design HD-720 format CMOS image sensor using SSLAR ADC technology. This task divided into four sub tasks. Commercially available IC fabrication processes will be evaluated for cost, sensor manufacturability, and IP portability. Based on the selection of the process technology architecture of the imager will be build. Architecture will be

Table 1. Project tasks, timeline, and resource allocation.

Project Timeline	Project Q1			Project Q2			Project Q3			Project Q4		
	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	June	July	Aug
Task 1: SSLAR Imager Design												
a. Technology evaluation and architecture design	x	x										
b. Block level integrated circuit design and simulation		x	x	x								
c. Integrated circuit (IC) block integration and verification				x	x							
d. Tapeout and fabrication (start on Jan. 30,2012)						x	x	x				
Task 2: Demo and Development Hardware and Software Design												
a. Demonstration and test board hardware design					x	x	x					
b. Software development							x	x	x		x	
c. System integration, debugging,and testing									x	x	x	
d. Development system design										x		
Task 3: Commercialization and Corporate Development												
a. Marketing strategy and product line planning						x	x	x	x	x		
b. Bussiness plan development and corporate building								x	x	x	x	x
c. Start-up company and product launch											x	x
Project Personale and Time Commitments	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	June	July	Aug
a. Project Lead (PI), Suat U. Ay	x	x	x	x	x	x	x	x	x	x	x	x
b. Research Assistant (RA, UofI graduate student)					x	x	x	x	x	x		
c. Peter Sutherland						x	x	x	x	x	x	x

divided into sub blocks, right before block level design starts. Layouts of the designed and simulated sub-blocks will be integrated to construct the whole imager IC. After final verifications it will be sent for fabrication (tapeout) in late January 2012. Right after the tapeout, second task will be initiated. In the second task demonstration and development hardware that the fabricated SSLAR imager will be mounted on along with the imaging software will be designed and fabricated. First the demo printed circuit board (PCB) will be designed. Software will be designed based on the SSLAR imagers control capabilities and the demo PCB features. Fabricated SSLAR imager ICs will be mounted on the demo system and both design and the software will be debugged and tested. Successful completion of these sub tasks will lead to the design of development system that could used for sampling the SSLAR imager to the future customers of the for-profit corporation that would have been founded. Project budget is shown on Table 2.

Table 2. Budget for the HD-720 SSLAR imager project

EXPENDITURES	*Project Q1*	*Project Q2*	*Project Q3*	*Project Q4*	Project
	Sept-Nov 2011	Dec.-Feb. 2012	Mar.-May 2012	June-Aug. 2012	TOTAL
Salaries/Wages					
Graduate Student (total 3 weeks in summer)	$ -	$ 2,500	$ 3,700	$ 1,000	$ 7,200
Fringe benefits (AY@1%, Sum@9%)	$ -	$ -	$ 100	$ 100	$ 200
Project Lead (total 3 weeks in summer)	$ -	$ -	$ -	$ 7,500	$ 7,500
Fringe benefits (Sum@24%)	$ -	$ -	$ -	$ 1,800	$ 1,800
Equipment and Software					
Cadence IC Design Software	$ 5,000	$ -	$ -	$ -	$ 5,000
PCB Design Software	$ -	$ -	$ 500	$ -	$ 500
Material and Supplies					
Printed circuit board manufacturing	$ -	$ -	$ 1,300	$ 1,500	$ 2,800
Parts and components	$ -	$ -	$ 1,200	$ 2,300	$ 3,500
(cable, ICs, optics, mechanics, etc.)					$ -
IC Manufacturing (Engineering Samples)	$ -	$ 20,000	$ -	$ -	$ 20,000
IC Packaging (30 packaged parts)	$ -	$ -	$ 1,500	$ -	$ 1,500
TOTAL	**$ 5,000**	**$ 22,500**	**$ 8,300**	**$ 14,200**	**$ 50,000**

Most of the tasks 2 and 3 will be carried in parallel. Mr Sutherland and UI-OTT will lead the task 3 while task 1 and 2 will be carried out by the project lead, Dr. Suat Ay and the UI graduate research assistant (RA) that will be hired during the second half of the project year.

Student RA and PI will work 3 weeks of in summer during this project. Large portion of the fund will be used for manufacturing the SSLAR imager in IC manufacturing facility. Designing and simulating of the imager circuits in task 1 and designing demo and development PCBs in task 2 required specialized software to be purchased. For task 1 Cadence IC Design Suite license will be purchased. For PCB design Eagle PCB Design software will be purchased. Projected PCB manufacturing and component purchases are also listed in the budget table.

CMOS active pixel sensor (APS) imagers have two main image readout architectures that provide these advantages. First one is called column series architecture that most of the low-end, and high-volume CMOS imaging devices are using. The high-end, high-speed CMOS image sensors take advantage of the second architecture called column parallel. Column parallel architecture (CPA) utilizes low speed, low-noise, on-the column analog domain processing and digitizer processors right after a row of pixels sampled on column level analog signal processing (CASP) circuits (Fig.1a). Four ADC types have been used in CPAs without degrading

competitive advantage of CMOS imagers. They are successive approximation (SA), integrating, delta-sigma, and cyclic type ADCs. Integrating type ADCs are also known as single or multiple slope ramp (SSR or MSR) ADC. Among the four ADCs, most noteworthy one is the SSR ADCs due to their advantages on multiple fronts when compared with others including ease of integration, smaller silicon footprint, low-power consumption, low-voltage operation, high bit resolution, low-noise operation, and low design complexity. They, however, suffer from operation speed especially when bit resolution is increased.

In the past, many solutions have been proposed to overcome the speed issue of SSR ADC. All methods try to reduce conversion time by means of using circuit and architecture design techniques. They generate digital codes that exactly map the effective pixel voltages to digital equivalents. They perform conversion blindly scanning all possible codes between 0 and 2n with n-bit digital counter and ramp (Figure.1c). If the code distribution of the sampled pixel

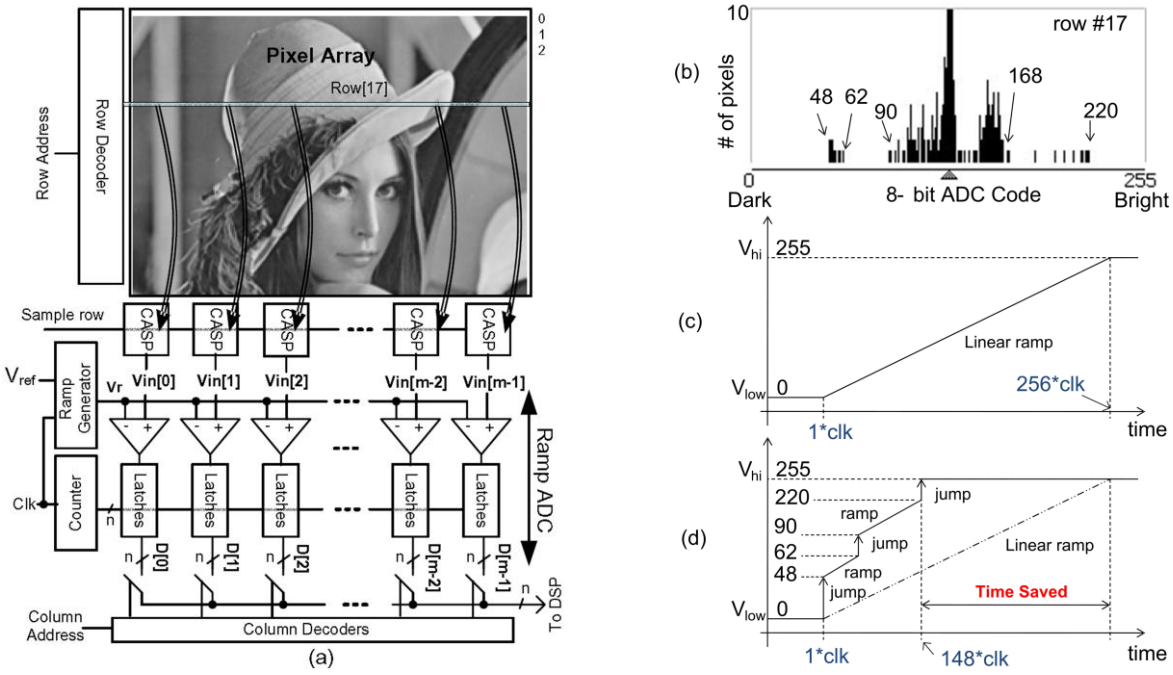

Figure 1. (a)A column parallel CMOS image sensor with integrated SSR ADC, (b) 8-bit code distribution of pixel signals on row #17 of captured image, (c) standard ramp ADC operation of pixel signals on row #17, (d) SSLAR ADC operation of pixel signals on row#17.

signals is known, on the other hand, some code ranges can be skipped on analog and digital domains resulting in improved conversion speed and reduced power consumption (Figure.1b,c,d). The SSLAR ADC technology exactly does this. It is a method to predict code distribution on the column of pixel signals, and an ADC algorithm to accelerate analog-to-digital conversion operation for column parallel CMOS image sensors.

The patent protected SSLAR technology was implemented on hardware achieving code range look-up, jump, and fall back operations on analog and digital domains as shown in Figure 2. Custom test board and imager boards were developed along with testing and viewing software as shown in Figure 2(b) and (c). Measurements showed that 10 times (10x) speed improvement could be achieved while power is reduced 10%with increased speed. As a result, we believe we have all necessary know-how to commercialize SSLAR technology.

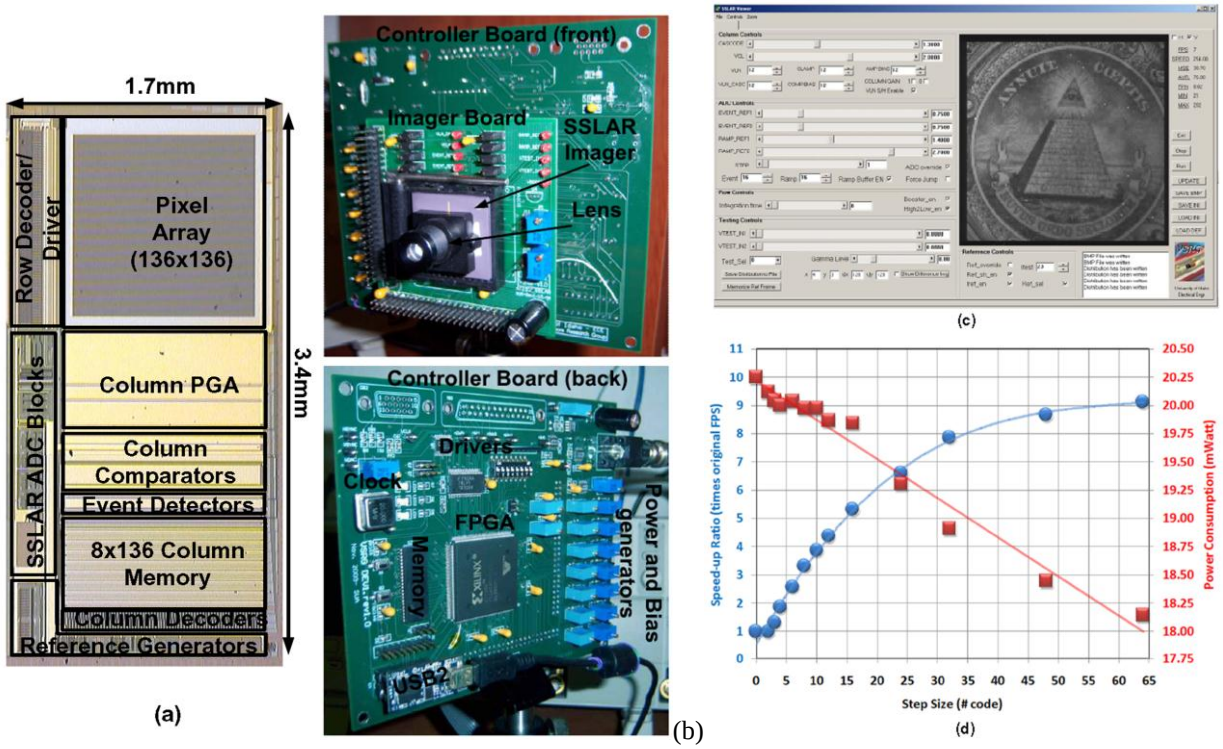

Figure 2. The SSLAR imager (a) die (b) development and test board, (c) test and viewing software, (d) measurement results showing speed up and power consumption of SSLAR imager.

7. Education and outreach: A graduate student research assistant (RA) will be hired to support hardware and software development. It is expected that the student will be the first hire of the newly founded company supporting demo and development systems, and may use the outcome of the project as his/her thesis work in completing their master of science (M.S.) study. It is also expected that the findings and performance metrics of the new SSLAR imaging technology will be disseminated to larger academic and commercial audience through journal and/or conference publication.

8. Institutional and other sector support: Mr. Sutherland will conduct market research and develop strategic partners to participate in the commercialization of the SSLAR technology. These strategic partners may be suppliers of the semiconductor chips, digital cameras or complete video surveillance systems. Mr. Sutherland will raise sufficient capital to build a robust capability to fabricate and market the chip sets or cameras.

Appendices

Appendix A. Facilities and Equipment:

The PI is an assistant professor in the Electrical and Computer Engineering Department at University of Idaho. He leads VLSI Sensors Research Group (VSRG) in same department. His group composes of graduate students who do research in the areas of mixed-signal VLSI design, low-voltage, low-power sensor electronics, and image sensors.

VLSI Sensors Research Group (VSRG) has a shared 500sqrf laboratory space furnished with computers and equipments to conduct research. Lab is equipped with Network/Spectrum Analyzer (0.01Hz and 1.8GHz), mixed signal oscilloscopes (100-500MS/s), pulse and arbitrary function generators (AFG3022B), precision multimeters (DMM4050), signal, voltage, and noise generators, and optical equipments such as a K-series TV Optoliner system, optical power meters, Oriel Cornerstone™ 130 1/8m Monochromator, lasers, optical tables, filters, and fiber optic light sources. It is also has high performance PC workstations that can run Windows and Linux operating systems for integrated circuit (IC) design and sensor characterization. Group develops in-house characterization and test software. VSRG group also have access to RF probe station and temperature chamber for integrated circuit (IC) testing under different temperature conditions.

PI will purchase no major equipment to successfully complete the project. Only item that will be outsourced will be the fabrication and packaging of integrated circuits (IC) containing envisioned self-powered imaging devices through a foundry service.

Suat Utku Ay, Ph.D.

Assistant Professor,
Electrical and Computer Engineering
University of Idaho at Moscow, ID, USA
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URL: http://www.ece.uidaho.edu/ee/analog/suatay/index.html

EDUCATION

- Ph.D. 2004 University of Southern California at Los Angeles. Electrical Engineering
- M.S. 1997 University of Southern California at Los Angeles. Electrical Engineering
- B.S. 1991 Yildiz Technical University at Istanbul, Turkey. Electronics and Telecomm. Engr.

PROFESSIONAL EXPERIENCE

- ASSISTANT PROFESSOR: Department of Electrical and Computer Engineering. University of Idaho, Moscow, Idaho, USA. Teaching and research in electrical and computer engineering, with research interests in mixed-signal VLSI design, analog electronics, VLSI sensors and interface design, semiconductor image sensors and electronics, reconfigurable electro-optical architectures for high performance computing, energy harvesting bio and photonic devices and systems, radiation hard electronics and imager design. (August 2007-present)
- SENIOR VLSI DESIGN ENGINEER AND ANALOG LEAD, Micron Technology Inc., Micron Imaging Division (now Aptina Imaging), Pasadena, California, USA, November 2001-July 2007. Some of the Micron CMOS image sensor products I involved in are; 2.0Mpixel (MT9D113), 3.0Mpixel (MT9T001), 5Mpixel (MT9P031), 8Mpixel (MT9E001), 1.3Mpixel, High Speed VGA (MT9V403).
- VLSI DESIGN ENGINEER, Photobit Technology Corp., Pasadena, California, USA, January 2001 – November 2001.
- ASSOCIATE VLSI DESIGN ENGINEER, Photobit Corp., Pasadena, California, USA September 1997 – December 2000.
- RESEARCH ASSISTANT, University of Southern California, Los Angeles, California, USA. Department of Electrical Engineering-Electrophysics, January 1998 – December 1998.
- TEACHING ASSISTANT, University of Southern California, Los Angeles, California, USA. Department of Electrical Engineering-Electrophysics, August 1996 – August 1997.
- RESEARCH/TEACHING ASSISTANT, Yildiz Technical University, Istanbul, Turkey. Department of Electronics and Telecommunication Engineering, August 1993 – May 1994.
- RESEARCH ASSISTANT, Yildiz Technical University, Istanbul, Turkey. Institute of Science, December 1991 – July 1993.

PUBLICATIONS

Dissertation

"*Design Issues and Performance of Large Format Scientific CMOS Image Sensor*", A dissertation submitted in partial satisfaction of the requirements for the degree of PhD in Electrical Engineering at University of Southern California at Los Angeles, December 2004, UMI Dissertation Services, Microform 3155375. (*Advisors*: Eric R. Fossum / John Choma)

Journal Articles

1. S. U. Ay, "*A Sub-1Volt 10-bit Supply Boosted SAR ADC Design in Standard CMOS*," An Intern. Journal of Analog Integrated Circuits and Signal Processing, vol. 66/2, pp. 213-221. Feb. 2011.
2. S. U. Ay, "*A compact power-on-reset pulse-generator (POR-PG) with low-power and wide operation range*", Journal of Circuits, Systems, and Computers (JCSC), Vol:19, Issue:6, pp.1365-1380, October 2010.
3. V. Sukumar, H. Hess, K. V. Noren, G. Donohoe, and S. Ay, "*Study on Threshold Patterns with Varying Illumination Using 1.3M Imaging System*," Journal of Intelligent Information Management, Vol. 2, pp. 21-25, January 2010.
4. S. U. Ay, "*Photodiode Peripheral Utilization Effect on CMOS APS Pixel Performance*" IEEE Trans. on Circuits and Systems-I, Reg. Papers, vol. 55, no. 6 ,pp. 1405-1411, July 2008.
5. S. U. Ay, M. P. Lesser, E. R. Fossum, "*CMOS active pixel sensor (APS) imager for scientific applications*," Proceedings of the SPIE, Volume 4836, pp. 271-278, 2002.

Conference Articles

1. A. Mesgarani, A. Tekin, S. U. Ay, "*A High-Speed and Low-Power Pipelined Binary Search Analog to Digital Converter*," 54th IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS), Seoul, Korea,7-10 August, 2011, (In press)
2. A. Mesgarani, S. U. Ay, "*A Single Channel 6-Bit 900MS/s 2-Bits Per Stage Asynchronous Binary Search ADC*," 54th IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS), Seoul, Korea,7-10 August, 2011, (In press)
3. S. U. Ay, "*Boosted Readout for CMOS APS Pixels*," IEEE International Symposium on Circuits and Systems (ISCAS), 15-18 May, 2011, Rio de Janeiro, Brazil (In press)
4. S. U. Ay, "*A 1.32pW/frame.pixel 1.2V CMOS Energy Harvesting and Imaging (EHI) APS Imager*" 2011 International Solid- State Circuits Conference (ISSCC), pp.116-117, 20-24 February 2011, San Francisco, CA, USA
5. A. Mesgarani, M. Alam, F. Z. Nelson, S. U. Ay, "*Supply Boosting Technique for low-voltage comparator design in standard CMOS*" 53nd IEEE International Midwest Symposium on Circuits and Systems, MWSCAS '2010, pp.893-896, 1-4 Aug. 2010, Seattle, WA, USA.
6. F. Z. Nelson, S. U. Ay," *Integration of a New Column-Parallel ADC Technology on CMOS Image Sensor*," IEEE Workshop on Microelectronics and Electron Devices, 2010. WMED 2010, pp. 1-4, 16 April 2010, Boise, Idaho, USA
7. A. Mesgarani, H. K. Sadeghi, S.U. Ay, "*Continuous-Time/Discrete-Time (CT/DT) Cascaded Sigma-Delta Modulator for High Resolution and Wideband Applications*"

IEEE Workshop on Microelectronics and Electron Devices, 2010. WMED 2010, pp. 1-4, 16 April 2010, Boise, ID.

8. S. Balagopal, S. U. Ay," *An on-chip ramp generator for single-slope look ahead ramp (SSLAR) ADC*," 52nd IEEE International Midwest Symposium on Circuits and Systems, MWSCAS '09, pp.: 373-376, 2-5 Aug. 2009, Cancun, Mexico.
9. S. U. Ay," *A nanowatt cascadable delay element for compact power-on-reset (POR) circuits*," 52nd IEEE International Midwest Symposium on Circuits and Systems, MWSCAS '09, pp.: 62 – 65, 2-5 Aug. 2009, Cancun, Mexico.
10. F. Z. Nelson, M. N. Alam, S. U. Ay," *A Single-Slope Look-Ahead Ramp (SSLAR) ADC for Column Parallel CMOS Image Sensors*," IEEE Workshop on Microelectronics and Electron Devices, 2009. WMED 2009, pp. 1-4, 3 April 2009, Boise, Idaho, USAS.
11. V. Sukumar, H.L. Hess, K.V. Noren, G. Donohoe, S. Ay," *Imaging system MTF-modeling with modulation functions*," Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, 10-13 Nov. 2008 Page(s):1748 - 1753
12. S.U. Ay, "*A hybrid CMOS APS Pixel for Wide-Dynamic Range Imaging Applications*", 2008 IEEE International Symposium on Circuits and Systems, ISCAS'08, May18-21,2008, Seattle, WA, USA.
13. S. U. Ay, E. R. Fossum "*A 76x77 mm^2, 16.85 Million Pixel CMOS APS Image Sensor with Large Pixel Well Depth*" 2006 Symposium on VLSI Circuits, June 15-17, 2006, Honolulu, Hawaii, USA
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