UNIVERSITY OF IDAHO
ELECTRICAL AND COMPUTER ENGINEERING

SSLAR Imaging System Development for High-Speed, High-Resolution Surveillance Camera Markets

Final Report

Suat U. Ay

6/27/2012

This is the final report for grant number IF12-015 for developing commercial grade, high resolution, high speed CMOS image sensor integrated circuit (IC) utilizing single-slope look ahead ramp (SSLAR) analog to digital converter (ADC) technology developed by the PI. Detailed specification, architecture, and circuits developed to realize high frames rate, high-definition (HD) image sensor in 720P format having nearly 1 million pixels (1292x732) are reported as well as developed test and demonstration systems for successful commercialization.

Table of Contents

A. Abstract

This report composes of the design and development details of commercial grade, high resolution, high speed CMOS image sensor integrated circuit (IC) utilizing patented single-slope look ahead ramp (SSLAR) analog to digital converter (ADC) technology. Detailed specification, architecture, and circuits developed to realize high-definition (HD) image sensor in 720P format having nearly 1 million pixels (1280x720) are reported as well as developed test and demonstration systems for successful commercialization.

B. Introduction

High-resolution, high-speed digital cameras are currently the fastest growing segment of the surveillance market worldwide. According to Frost & Sullivan (F&S), the worldwide digital camera market is expected to grow by more than 20% per year from $2.7 billion USD in 2010 to $4.8 billion by 2016. Most major image sensor companies are developing new digital video camera product lines to capture a portion of this market. They typically do this by expanding their current product lines that were originally optimized for the high-volume, low video rate (15-30 frames/s) consumer markets, such as cell phones and digital still cameras. The main dilemma companies are facing is to balance return of investment, design risk, and meeting the surveillance market demand for 1) high resolution (720p HD or better), 2) low-power consumption (<250mW), and 3) high-frame rate (>120frames/s) imaging. For a typical image sensor company, addressing resolution is not a problem. However, using current circuit Intellectual Properties (IP) for the new designs does not address the low-power and high speed operation requirements for advanced digital cameras surveillance applications. This forces companies to develop a new product line investing heavily on new design techniques, technologies, and circuit IP which increase risk and effect profitability. Seeing an opportunity, the PI has developed a patent protected algorithm and circuit IP that addresses the need for speed and low-power consumption, all without sacrificing image quality. Called the single-slope look-ahead ramp (SSLAR) analog-to-digital converter (ADC) technology, it is designed to meet this market demand for high-speed, high-resolution, and low-power camera systems. SSLAR ADC technology scales linearly (in terms of bit-resolution and power consumption) as opposed to the current ADC technologies used in CMOS image sensor thereby reducing design risk. PI has already designed and fabricated integrated circuits (IC) that prove the effectiveness of the SSLAR technology under laboratory conditions.

C. Project Goals and Achievements

Three specific tasks identified to achieve the goals during this project were:

1. Design and fabrication of a commercial grade HD-720 format SSLAR imager sensor IC.
2. Integration of the designed SSLAR imager IC into a demonstration and development system with commercial grade software and hardware.
3. Develop a business plan for successful commercialization of the SSLAR technology and fund a for-profit corporation spinning off SSLAR IP from UI.

C.1 The SSLAR Technology

CMOS active pixel sensor (APS) imagers have two main image readout architectures that provide these advantages. First one is called column series architecture that most of the low-end, and high-volume CMOS imaging devices are using. The high-end, high-speed CMOS image sensors take advantage of the second architecture called column parallel. Column parallel architecture (CPA) utilizes low speed, low-noise, on-the column analog domain processing and digitizer processors right after a row of pixels sampled on column level analog signal processing (CASP) circuits (Fig.1a). Four ADC types have been used in CPAs without degrading competitive advantage of CMOS imagers. They are successive approximation (SA), integrating, delta-sigma, and cyclic type ADCs. Integrating type ADCs are also known as single or multiple slope ramp (SSR or MSR) ADC. Among the four ADCs, most noteworthy one is the SSR ADCs due to their advantages on multiple fronts when compared with others including ease of integration, smaller silicon footprint, low-power consumption, low-voltage operation, high bit resolution, low-noise operation, and low design complexity. They, however, suffer from operation speed especially when bit resolution is increased.

In the past, many solutions have been proposed to overcome the speed issue of SSR ADC. All methods try to reduce conversion time by means of using circuit and architecture design techniques. They generate digital codes that exactly map the effective pixel voltages to digital equivalents. They perform conversion blindly scanning all possible codes between 0 and 2n with n-bit digital counter and ramp (Fig.1a). If the code distribution of the sampled pixel signals is known, on the other hand, some code ranges can be skipped on analog and digital

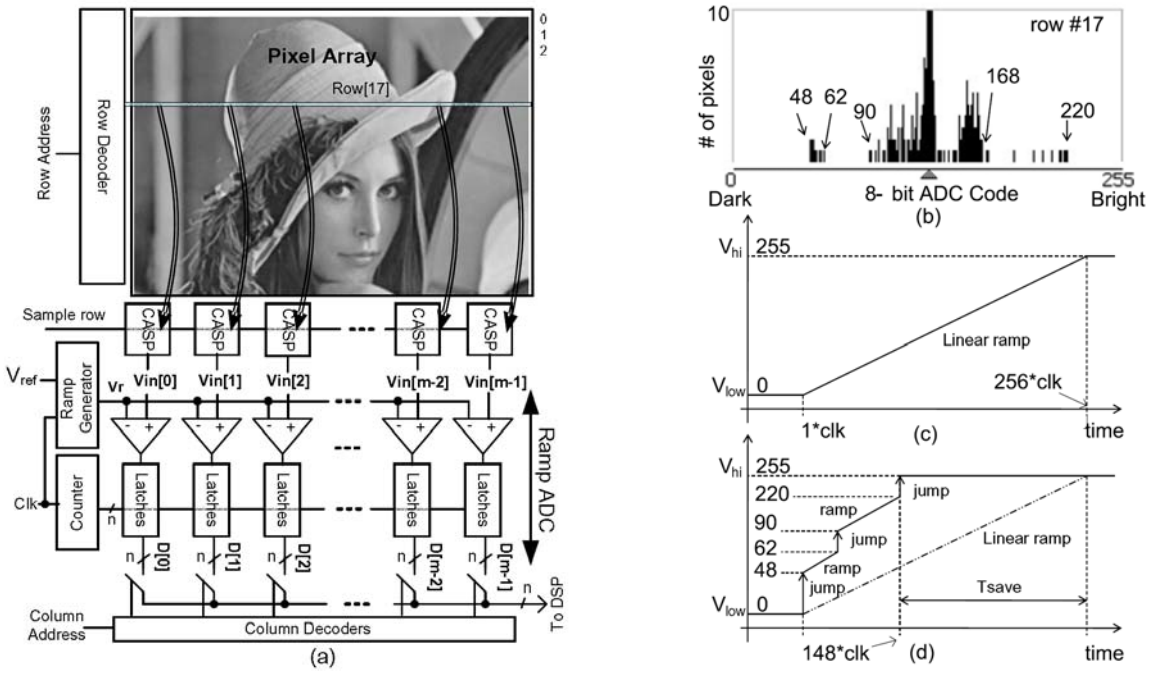


Figure 1. (a)A column parallel CMOS image sensor with integrated SSR ADC, (b) 8-bit code distribution of pixel signals on row #17 of captured image, (c) standard ramp ADC operation of pixel signals on row #17, (d) SSLAR ADC operation of pixel signals on row#17.

domains resulting in improved conversion speed and reduced power consumption (Fig.1b,c,d). The single slope look-ahead ramp (SSLAR) ADC technology exactly does this. It is a method to predict code distribution on the column of pixel signals, and an ADC algorithm to accelerate analog-to-digital conversion operation for column parallel CMOS image sensors.

C.2 The SSLAR Algorithm

As mentioned in previous section, if the digital code distribution of input analog voltages is known, ramp ADC operation can be modified and accelerated. This look-ahead or prediction operation can be done instantaneously in ideal case. However, in reality prediction requires a computation time in terms of number of clock cycles or h clock cycles every time look-ahead operation is performed. Another deviation from ideal look-ahead operation is that we need to consider how can we quantify or say that there is not enough number of columns drop in the look-ahead code range. A look-ahead range and a threshold have to be used in real circuit implementation to make a judgment resulting in code jump ahead or fall back operation. Thus, code look-ahead range both in analog and digital domain has to be set to a reasonable range, and number of columns dropping in this range has to be counted and compared against a threshold level. In SSLAR algorithm code look-ahead range is called step size (k) and threshold is jump threshold (s).

Block diagram of the single slope look-ahead ramp (SSLAR) ADC architecture for column parallel CMOS image sensors is shown in Fig. 2. Comparing with a typical SSR ADC shown on Fig.1, SSLAR ADC has one extra block called predictor on each column, modifier global ramp generator and counters, an event detector, and a global look-ahead controller (LAC) blocks to implement SSLAR ADC algorithm. Modified ramp generator and counter could be able to jump k-step and k/2-code ahead from their current voltage or code level, respectively. They also accommodate fall back of k-step and k/2-code if jump operation is not approved by the LAC block. Function of the predictors is to generate a signal collectively, informing LAC block about the number of column comparators that changed state during look-ahead operation. Based on these extra blocks and operation

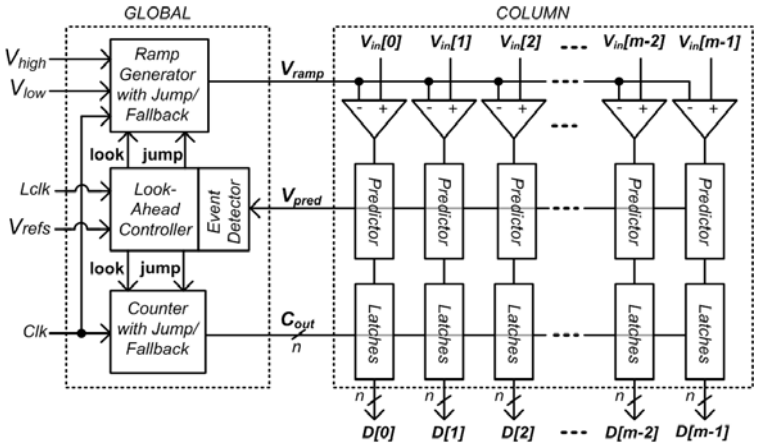


Figure 2. Column-parallel integration of single-slope look-ahead ramp ADC.

principles, SSLAR ADC implements the algorithm steps given in Table I.

Analog to digital conversion of m-number of CASP signals performed at the same time on column parallel architecture. After a row of pixel signals sampled on CASPs, and global ramp and counter circuits are reset, conversion starts with looking ahead k-step. Before look-ahead operation, LAC initializes event detector and asserts jump signal. Before ramp voltage is increased, counter code is incremented (k/2)-LSB, and let column latches to pass this level first. Next, ramp voltage is increased k-LSB equivalent voltage given with (1).

$$\Delta V_{ramp} = k \cdot \left(\frac{V_{high} - V_{low}}{2^n} \right) \tag{1}$$

Right after ramp and counter signal settled on their jump levels, event detector will process the column predictor outputs quantifying number of comparators that changed states due to the jump performed by the ramp generator. If any of the m voltage inputs ($V_{in}[i]$) is in between V_{ramp} and $V_{ramp}+\Delta V_{ramp}$ range, then their comparator outputs will change state from logic-1 to logic-0. This change will be detected by the column predictors and a single signal is sent to event detector. At the same time column latches will lock on the counter's current output if the control input from comparator is changed from 1 to 0. At this point LAC will receive the number of column comparators that changed state (z) and will compare this number with the jump threshold (s). If the z is smaller than s, then LAC will approve jump operation incrementing counter another k/2-LSB. What this means is that there might be a number of column voltages (z) exist falling in between the k-LSB look-ahead range, but, they are less than the threshold (s) that was set. In this case, SSLAR algorithm blindly quantizes these z numbers of column voltages uniformly with value equals to previous code plus k/2-LSB, or the mid-code ($C_{out}+k/2$). This will cause a quantization error or noise. Total quantization error for entire row can be given with (2) for the worst case situation in where all the columns in every k-step look-ahead operation have same voltage levels, and located at the far end of the look-range.

TABLE I. Single-Slope Look-Ahead Ramp (SSLAR) ADC Algorithm

Step		OPERATION
1		Sample a row of pixel signals on column ASP circuits
2		Reset global ramp generator and n-bit counter
3		Initialize column predictors for possible jump operation
4		Increment global counter (k/2)-LSB
5		Increase ramp voltage k-LSB equivalent analog level
6		Check column predictors
7		Are there enough column comparators changing their outputs in k step range?
	A	If YES: Fall back k-LSB on ramp voltage and (k/2) step on counter output. Ramp and count 1-LSB at a time for k-LSB, then go to Step 8.
	B	If NO: Do not change analog ramp voltage, increment counter (k/2) step more, go to Step 8
8		Have you reached 2^n-1 bit range? If NO, go to Step 3, If YES, go to Step 9
9		Have you read all *m* rows? If NO, increment row address, go to Step 1, If YES, end of frame.

$$E_{row} = \frac{k}{2} \times \sum_{j=1}^{\frac{m}{k}} z_j \tag{2}$$

where k is an even number representing jump step size, and m is the number of columns. If the z is larger than or equal to s, then LAC will disapprove jump operation, due to that fact that many columns exist in the look range, and assigning the mid-code for all pixels will result in large quantization error. Thus, it will force ramp to fall back k-step, and counter to fall back k/2-LSB. It then ask ramp generator and counter to increment one LSB at a time for k-steps during the next k clock cycles.

These two cases that jump is approved and denied are depicted in Fig.3. In the case when jump is approved, (k-h) clock cycle is saved. If it is denied, however, h clock cycles would be lost. In worst case, this will slow down the conversion operation. In best case, however, all column voltages will be in one k-step range of the SSLAR ADC (Vin[0..m-1]~Vx). This is the case that could be observed for the first few rows seen on Fig.1. Worst case is observed when there are more than threshold number of pixel signals exists on every k-step range of the SSLAR ADC. This is the case when sampled image have gradient intensity variation across the scene covering full ADC range and s<k. Conversion time of SSLAR ADC can be calculated for best and worst cases with the equations (3) and (4), respectively.

$$T_{SSLAR,Best} = \left(\frac{2^n}{k} \cdot h + k \right) \cdot T_{clk} \tag{3}$$

$$T_{SSLAR,Worst} = \left(\frac{2^n}{k} \right) \cdot (h + k) \cdot T_{clk} \tag{4}$$

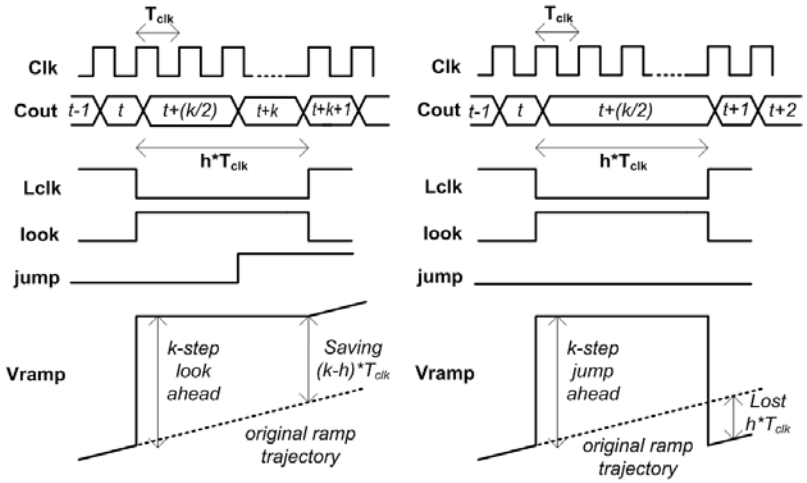


Figure 3. Timing diagram of LAC, counter and ramp generator blocks of SSLAR ADC a) jump is approved b) jump is denied

For all cases, standard single-slope ramp (SSR) ADC have same conversion period of 2n clock cycles. To quantify speed-up (Rsup) with the new ADC algorithm, conversion time of the SSR ADC is normalized with the conversion time of the SSLAR ADC for best and worst cases. It is given with (5).

$$R_{\sup} = \frac{T_{SSR}}{T_{SSLAR}} = \begin{cases} \left(\dfrac{k}{h + k^2 \cdot 2^{-n}} \right) & Best \\ \left(\dfrac{k}{k+h} \right) & Worst \end{cases} \tag{5}$$

Average speed-up ratio (Rsup) in where half of the pixel signals have worst case pattern, and the half has the best is plotted in Fig. 4 for 10-bit SSLAR ADC for different h and k values. h is the cost of look-ahead operation, and could be 1, 2, or 3 clock cycles. For this particular case, SSLAR algorithm could result in at least six times speed improvement. One of the important features of the SSLAR algorithm is that, it works like a regular SSR ADC if the step size (k) and threshold (s) is set to 1 LSB. In this case however, SSLAR ADC works slower then SSR ADC as seen in Fig.4. This feature allows us to evaluate SSLAR ADC algorithm on same focal plane in terms of speed-up ratio and noise level or image quality degradation.

C.3 SSLAR Imager IC Design

C.3.1 Column Analog Signal Processor (ASP) Circuits

The analog signal processing circuits from pixel photodiode (PD) node to digital outputs are shown in Fig.5. 3T CMOS APS pixel composes of the reset (M_1), select (M_3) and source follower (M_2) transistors. Column analog signal processor (ASP) composes of a programmable charge amplifier (A_1) which performs correlated double sampling (CDS) and a sample and hold circuit composing of SH switch and C_1 capacitor. Bottom plate of C_1 is connected the analog ramp signal bus. Amplified effective pixel voltage (ΔV_{SH}) is sampled and hold at the input of

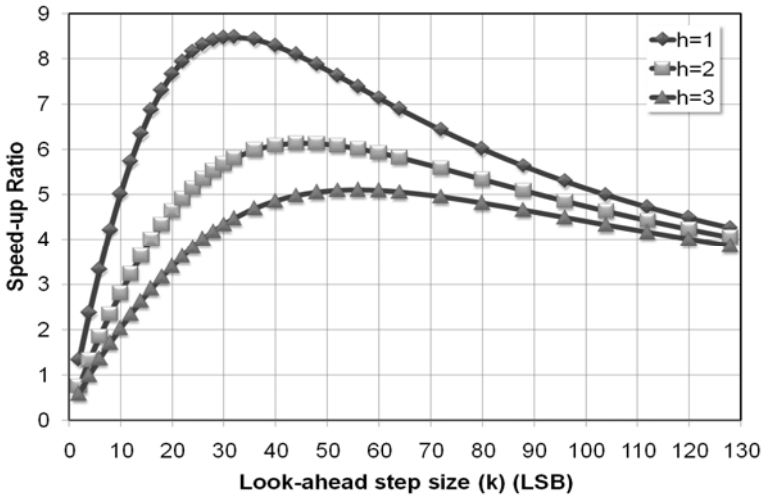


Figure 4. Average speed-up ratio of SSLAR ADC

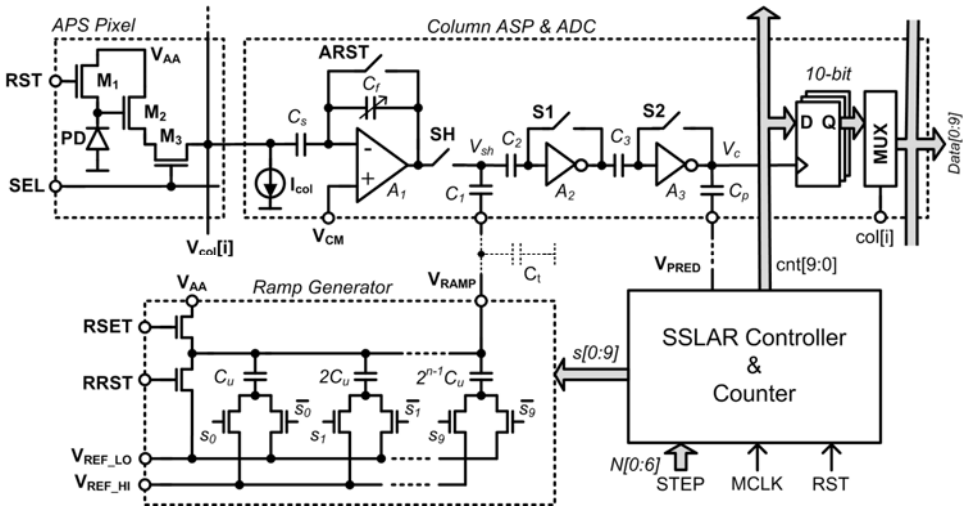


Figure 5. Column ASP and ADC circuits of the SSLAR imager.

the ADC comparator with respect to the clamp voltage, VCM. It is given in (6).

$$\Delta V_{SH} = V_{CM} - A_{SF} \cdot \left(\frac{C_s}{C_f} \right) \cdot \left(V_{PD,rst} - V_{PD,sig} \right) \tag{6}$$

Here, ASF is the gain of pixel source follower, $V_{PD,rst}$ is the photodiode reset voltage, and V_{PDsig} is the photodiode signal voltage. ADC comparator is formed by two inverting amplifiers (A_2 and A_3), offset nulling capacitors (C_2 and C_3), and switches (S_1 and S_2). Column predictor composes of a single capacitor, C_P. It is connected between the output of the comparator and the global event detector bus (V_{PRED}). Comparator output is connected ten transparent data latches. Latches pass the global counter signals when the comparator output is low, and hold last known inputs when it is high. Timing diagram of the readout chain is shown in Fig.6.

Global binary weighted ramp generator is directly coupled to the column ASP through the sample and hold

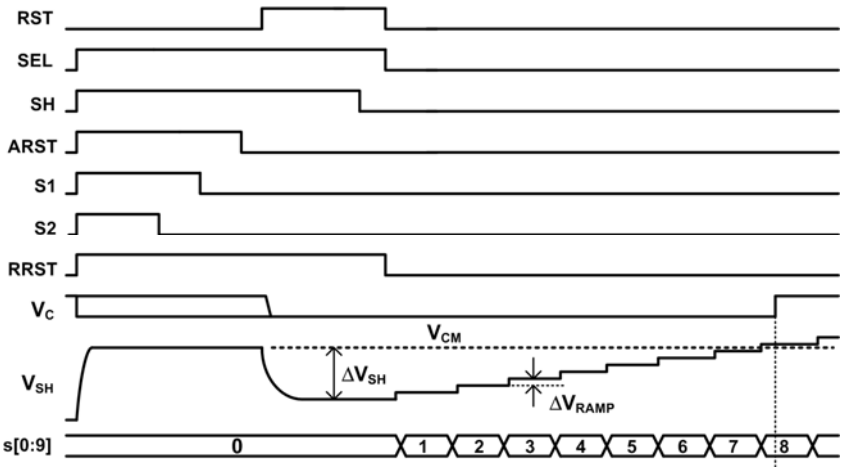


Figure 6. Timing diagram and associated node signals of the ASC and ADC

capacitor, C_1. A voltage buffer was not used to drive ramp generator voltage for saving power in the design. The ramp driver is the main power consuming circuit in a typical SSR ADC used in image sensors due to the large parasitic load (C_t). This capacitor is proportional to the number of columns (m) and the size of the effective column sample and hold capacitor of the imager.

Assuming the input capacitance of the comparator amplifier A_1 is much smaller than the nulling capacitor C_2, the ramp step size can be found by using (7).

$$\Delta V_{RAMP} = \frac{C_u \cdot \left(V_{REF\_HI} - V_{REF\_LO}\right)}{\left(2^n - 1\right) \cdot C_u \cdot \left(1 + \frac{C_2}{C_1}\right) + m \cdot C_2} \tag{7}$$

Here, n is the number of ADC bits, m is the number of columns, and Cu is the unit capacitor used in the ramp generator. In our design, we used ΔV_{REF}=2.5V, C_u=50fF, C_1=520fF, C_2=260fF, n=10, and m=200. Thus the minimum ramp step was 0.97mV with 10-bit resolution with 1V ADC input range.

C.3.2 Global SSLAR ADC Blocks

Global section of the SSLAR ADC composes of three blocks; SSLAR controller (CONT), event detector (ED) and ramp-count generator (RCG) as shown in the Fig.7. Controller block implements the SSLAR algorithm using the feedback from event detector. It also generates control and clock signals for the RCG blocks. Look-up threshold (s) was implemented in analog domain using two bias voltages to the event detector while the look-up step size (k) is applied by the user. 10-bit SSLAR ADC was designed with 7-bit look-ahead step size control (N[6:0]).

C.3.3 Event Detector Design

The event detector (ED) composes of a high-speed open loop comparator and a CMOS switch, as shown on Fig.8. The ED is connected to column predictor capacitors and generates the “jump” signal after “look” signal is asserter by the SSLAR controller. When “look” is high, analog predictor bus (V_{PRED}) is reset to V_{ER1}. When “look” signal is high analog ramp signal is frozen while ramp counter increments 1 or k/2 bits. During this time period none of the column comparator outputs change state. When “look” is asserted low, analog ramp signal rise 1 or k

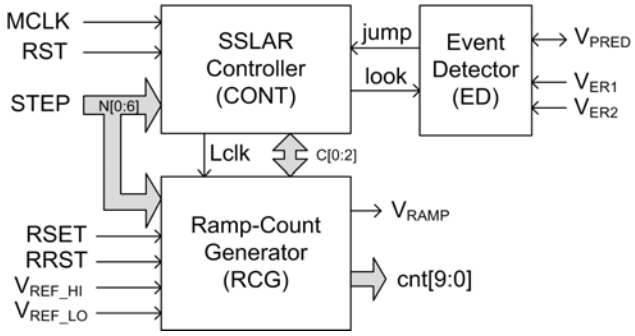


Figure 7. Global SSLAR ADC blocks.

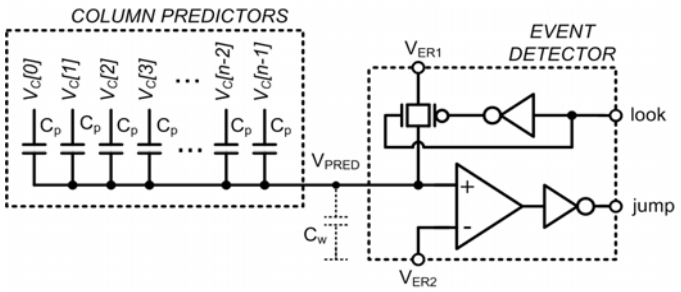


Figure 8. Event detector circuits.

step equivalent voltage causing b number of column comparators to change state from low to high. As a result of this, predictor bus voltage increases as given in (8).

$$\Delta V_{PRED} = \frac{z \cdot C_P \cdot V_{AA}}{(m-z) \cdot C_P + C_W} \tag{8}$$

Here, z is the number of column comparators that changes their state due to the look-ahead ramp operation. If ΔV_{PRED} is larger than the (V_{ER2}-V_{ER1}) difference then event detector pulls "jump" signal high confirming that the number of columns that are in the look-ahead step range (k) is less than the desired threshold number of columns (s), and let the SSLAR controller block that the jump operation is approved. Thus, for given threshold number of columns (s), the two event reference voltages have to be adjusted as given in (9).

$$V_{ER2} = V_{ER1} + \frac{s \cdot C_P \cdot V_{AA}}{(m-s) \cdot C_P + C_W} \tag{9}$$

In out design m=200, V_{AA}=3.3V, C_p=50fF, and C_W=400fF. For example, for s=2 results in event detector bias difference of 32mV defining the required accuracy of the comparator used in the event detector.

C.3.4 SSLAR Controller (CONT) Design

SSLAR controller unit is the central part of the SSLAR ADC. It generates unique control signals for ED and RCG blocks implementing the SSLAR ADC algorithm. Internal making of the controller unit is shown in Fig. 9. The finite state machine (FSM) implements the algorithm while 7-bit synchronous counter and digital comparators are

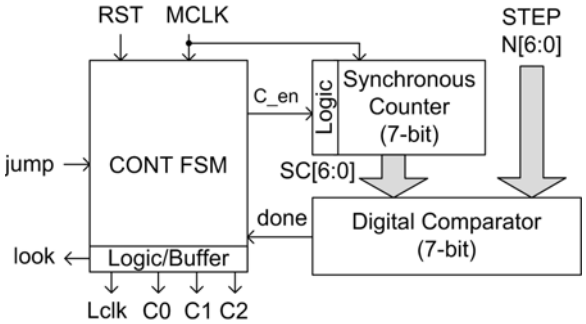
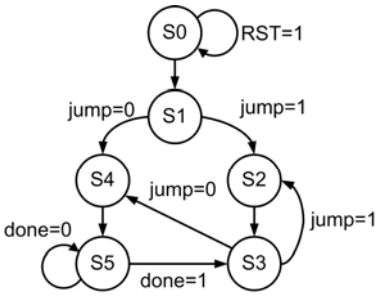


Figure 9. Block diagram SSLAR ADC controller unit (CONT).



State	Look	C0	C1	C2	C_en	RST
Sx	1	0	1	0	0	1
S0	1	0	1	0	0	0
S1	0	1	0	1	0	0
S2	1	1	0	0	0	0
S3	0	1	0	1	0	0
S4	1	0	0	0	0	0
S5	1	0	1	0	1	0

Figure 10. Finite state machine (FSM) diagram and the state assigned outputs of the SSLAR controller unit.

used when jump operation is not approved, incrementing the analog and digital ramp 1 bit at a time. The controller FSM is shown in Fig. 10. It has six (6) operation states to generate five different control signals as listed in Table II. Some of the signal are used directly by the ED and RCG units (Look, Cnt[2:0]), while some of them are used internally to generate other control signals.

Four control inputs signals define the state of FSM. These signals are: ADC reset (“rst”), jump signal from event detector (“jump”), internal counter done signal (“done”), and master clock signal (“mclk”). If the rst=1, state machine stays at S0 state. The FSM changes its state at rising edge of the master clock signal conditionally or unconditionally. Unconditional state changes only exist from states S4 to S5 and from S2 to S3. Other state transitions depend on the inputs jump, done and reset. If the reset is set high, state machine goes to state S0 and waits until the reset signal is cleared to move to state S1. Done signal is generated in the CONT unit by a 7-bit synchronous counter and comparator units. Operation of the counter/comparator combination is enabled by the FSM through counter enable signal (C_en). If C_en=1 then the counter start counting while comparator checking weather counter value (SC[6:0]) is equal to the look-ahead step (N[6:0]). If it is equal it asserts the done signal to high for FSM to take action. If done signal is asserted high, then the counter enable signal is de-asserted (C_en=0), and changes the state from S5 to S3. When C_en=0, synchronous counter is reset to “0000000”, waits for C_en to be asserted high again. Logic attached to the counter is used gating and delaying certain signals for proper operation.

C.3.5 SSLAR Ramp-Counter Generator (RCG) Design

Block diagram of the ramp-count generator unit is shown in Fig. 11. It generates the analog ramp signal and 10-bit digital counter outputs. Unit composes of two multiplexers, one carry-look ahead (CLA) full-adder, 10-bit full adder latches (FAL), two carry-look ahead digital subtractors, one 10-bit binary weighted charge scaling ramp generator, and deglitching digital buffer blocks. Look ahead, jump and fall back operations are controlled through the proper timing of the blocks without having synchronous counter units in the RCG unit. Only clocked unit is the 10-bit latches unit which allow programmable look-ahead, jump or fall back operations.

The CLA full-adder, full-adder latches (FAL), and the logic blocks are the central part of look-ahead and jump operation. Latch clock (Lclk) is generated in the CONT unit. 10-bit inputs (W0[9:0]) to CLA full-adder are

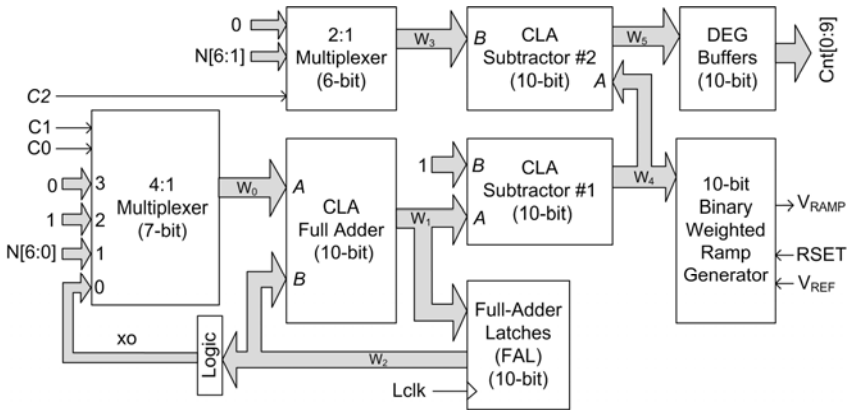


Figure 11. SSLAR ADC ramp-count generator unit block diagram

provided by the 4:1 multiplexer unit. Other inputs (W2[9:0]) are came from the 10-bit latch outputs. Rising edge triggered D-type flip-flops were used in the FAL unit.

Depend on the state of the FSM in CONT unit, one of the four words are passed to CLA unit from 4-to-1 multiplexer using inputs C1, C0. When inputs are “00”, digital word containing xo at LSB bit applied to CLA full-adder. If it is “01”, then the 7-bit step programming word (N[6:0]) is passed. Digital word equal to one (000000001) is passed when the inputs are”10”, and zero is passed when the inputs are “11”. As a result, CLA full-adder outputs (W1[9:0]) behaves like a 10-bit counter. It either stops counting for “11”or increments one LSB at a time for “10”, or counts n-by-n (N[6:0]=n, i.e. n=5 if N[6:0]=”0000101”) for “01”. Logic block generates xo signal using a 10 inputs NOR gate.

Carry look-ahead type adder was used for reducing glitches at the counter outputs which was used directly by the binary weighted ramp generator (BRG) block. Carry-look ahead subtractor #1 block subtracts “00000001” from the CLA block outputs (W1[9:0]). This allows digital bits used by BRG to be between 0 and 1023 for 10-bit. This is due to the fact that CLA generates counter output between 1 and 1024.

2-to-1 multiplexer passes the half step programming word if C2=’1’ or the zero (‘0’) to the subtractor#2. It implements the half and full step counter increment operations of the SSLAR ADC algorithm. Half of the step code word is obtained by using upper 6 bits of the original step program word as multiplexer input. CONT FSM was designed such a way that half step word is not subtracted from the first subtraction unit outputs (W4[9:0]) during the first look-ahead operation at which CLA outputs (W1[9:0]) equal to “0000000001” and first subtractor output (W4[9:0]) is “0000000000”.

An 8-bit operation of the SSLAR ADC with forced jump input from ED block is shown in Figure 12. In the simulation, jump input is forced to allow code jump operation all but one 16-LSB code range between 112 (01110000) and 127 (01111111). Ramp low and ramp high levels were set to 1.0 and 2.0 volt. Analog ramp voltage increased 62.5mV or 16LSB equivalent voltage during look-ahead ramp operation. If jump is approved, it maintains the jump voltage and looks-ahead again. If jump is denied, then ramp voltage falls back, and

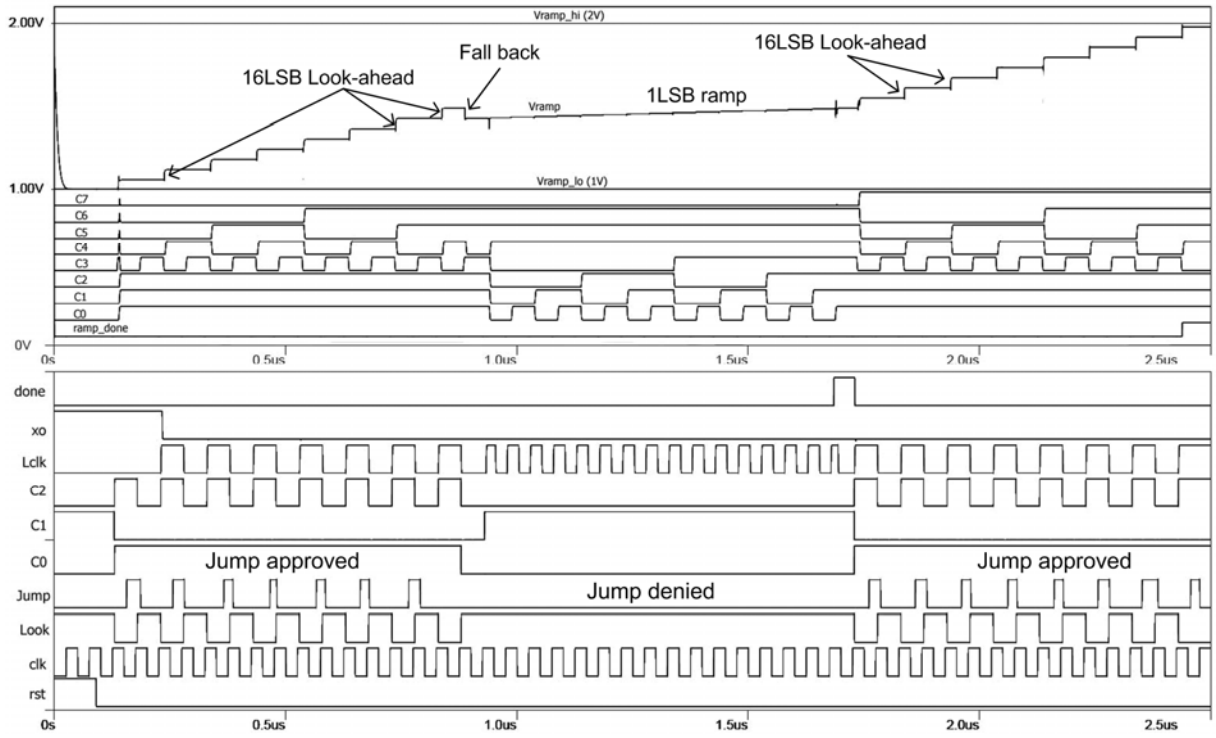


Figure 12. 8-bit full block simulation results of the SSLAR ADC's controller and ramp-count generator unit with step=16LSB, and jump signal is forced.

increments 1LSB equivalent voltage or 3.906mV. At the end of the single step operation it looks-ahead again and this operation continues until full 8-bit code range is scanned.

C.3.6 HD-720P Format Integration of SSLAR ADC

Given the die size constraints set by the total cost of fabrication, HDTV 720p format was chosen in this project. Thus the total number of pixels on x- and y-direction were 1280 and 720, respectively. As a barrier and signal processing purpose, 12 extra rows and column of dark pixels were also added. As a result total number of pixels in the design becomes 1292 x 732 totaling 945,744.

The SSLAR imager was designed and fabricated in a 0.18μm CMOS process. Standard 3T CMOS APS pixel with 3.2μm pixel pitch was integrated in the pixel array. To maintain the frame rate, two-side architecture was adopted. For every row sampling period, two rows of pixels were sampled. Odd columns on even rows and even column on odd rows were sampled on the bottom SSLAR ADC while the odd columns on odd rows and even column on even rows on the top. This allows green pixels to be read through same circuits on bottom signal path while red and blue pixels on the top. To improve the matching and size of column circuitry, single programmable charge amplifier was used on each side. Two SSLAR ADC channel are integrated on each side composing of two comparators and two 12-bit transparent SRAM blocks. To reduce the column readout time, even and odd columns composing of two ADCs were scanned separately on each side resulting in four parallel readout channels for the architecture. ADC resolution is programmable and could be either 10-bit or 12-bit.

Default is 12-bit operation. Single SSLAR controller was used on each side reducing size, power, and complexity of the architecture. Symmetric layout is critical to reduce matching for top and bottom channels. Thus, reference voltage and currents are generated on the middle right side of the chip and distributed top and bottom side from the middle. Bias voltages and currents were generated on top and bottom side independently. A serial scan chain was included in the design to control voltages and currents of individual blocks. Scan chain also used to program and control the SSLAR ADC core and digital control block in the design. On chip digital block was synthesized and implemented for the design. To achieve first time silicon success, digital control block was designed to be overridden by control inputs through the pads. As a result number of pads used in the design become 120. Out of 120 pads, 52 of them are the digital outputs of the four 12-bit channels plus synchronization signals for top and bottom sides.

Micrograph of the designed imager IC is shown in Fig.13. Chip size is 4.85mm on x-direction and 4.05mm on y-direction totaling 19.64mm^2. It composes of 120 pads for bonding on the IC package. For testing and demonstration two different packages were acquired. Ceramic PGA 120 type package will be used for testing the IC while ceramic QFP 120 will be used for demonstration. Custom made aluminum boxes will be used for housing the demonstration camera while standard CCTV C-mount camera lenses will be mounted on the camera box. IC packages, lenses, and aluminum boxes has been acquired and made ready for testing and demonstration.

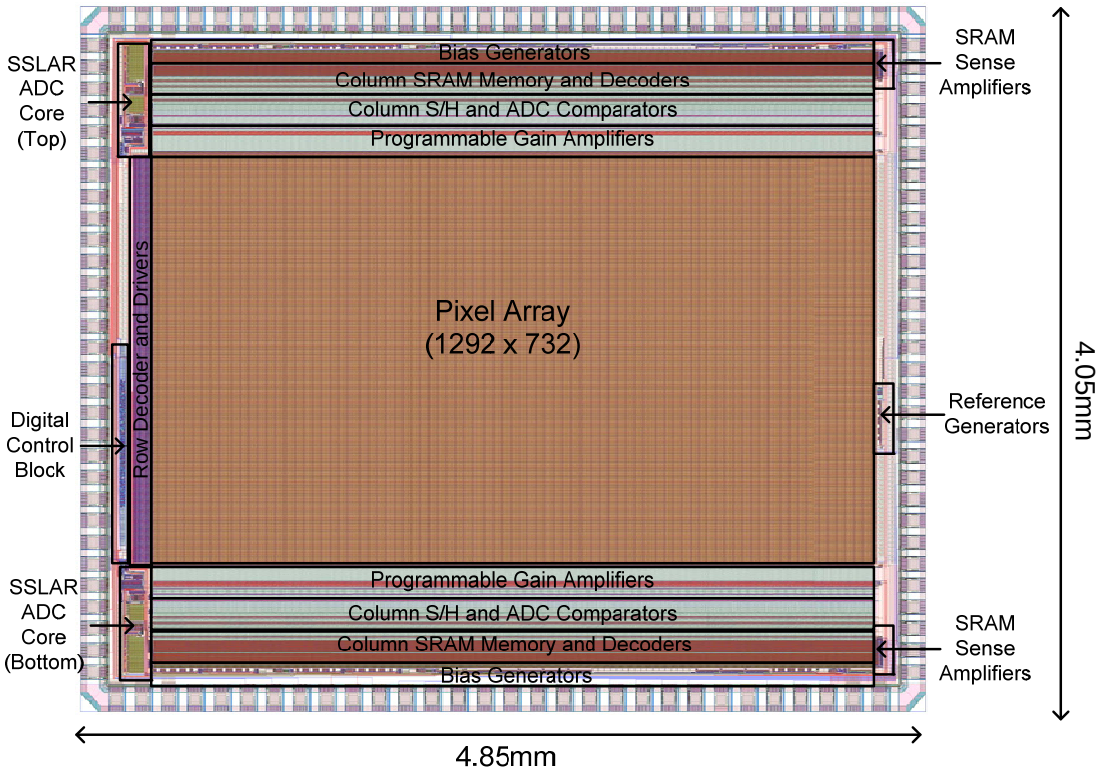


Figure 13. SSLAR chip micrograph.

C.3.7 Operation Modes

One important feature of the SSLAR ADC is that it can work as a standard SSR ADC without any speed penalty when jump signal is overridden externally and by setting look-ahead step size to 1LSB. By changing step size to 2, 4, and 8LSB reduce the 12-bit ADC resolution to 10, 8, and 6-bit, respectively, effectively trading speed (and power consumption) with the resolution. Besides, SSLAR controller also could be programmed to operate 10-bit resolution instead of 12-bit, speeding up the operation trading the resolution. The SSLAR ADC architecture also allows resolution change on the fly allowing high resolution acquisition of predefined regions or rows on the pixel array.

Frame rate is depends on the SSLAR ADC speed-up ratio and typically 4x to 6x speed-up ratio is expected from a typical scene image. This results in the worst case frame rates between 30 FPS to 80 FPS for 12-bit operation of the SSLAR ADC as shown in Fig 14.

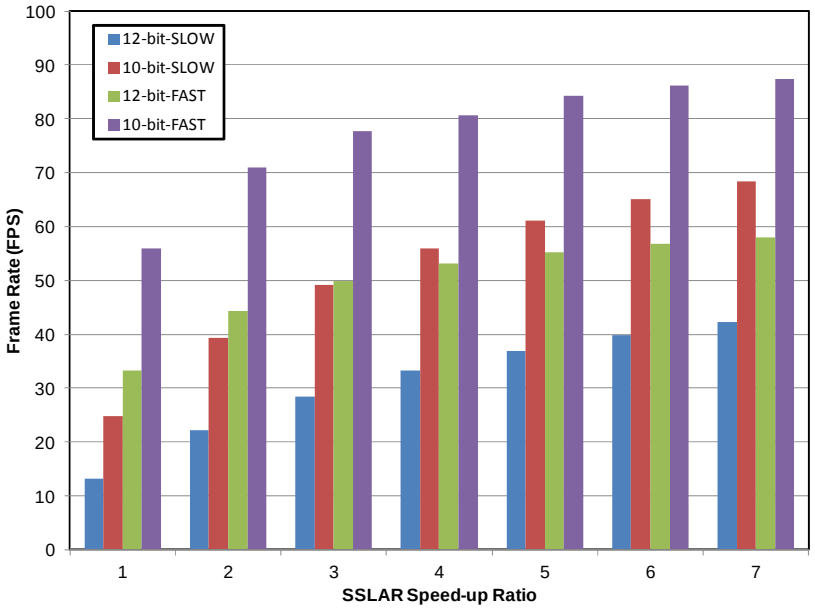


Figure 14. Frame rates versus SSLAR ADC speed-up ratio for different operation modes.

C.3.8 Test and Demonstration Platforms

Testing and demonstration platforms will have two different printed circuit board (PCB) circuitry. Test platform will have more flexible architecture to be able override the internal digital block of the IC while storing and sending the frames properly. Test platform will also be used for fixing the firmware of the demonstration board. Schematic, layout, and assembled test board for the SSLAR chip is shown in Figure 15. Test board composes of logic level shifters, USB2 communication IC, voltage regulators, high speed flash memories, reference DACs, and FPGA for timing and control signal generation. The test and demonstration software was written to accommodate large format image viewing and analysis as shown on the Fig. 16.

Demonstration board and its firmware will be assembled after the testing is completed.

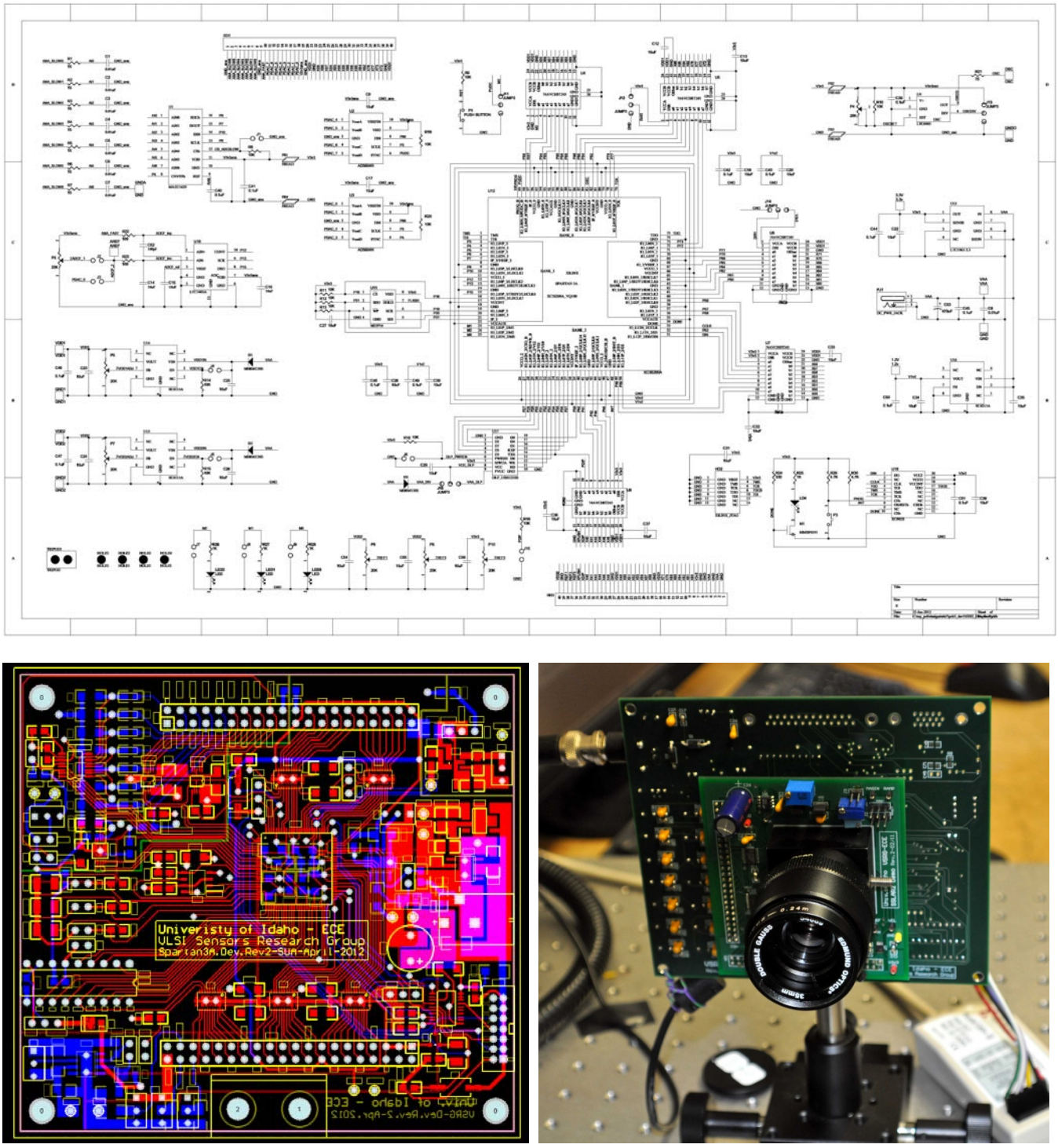


Figure 15. Test board schematic, layout, and assembled board for testing.

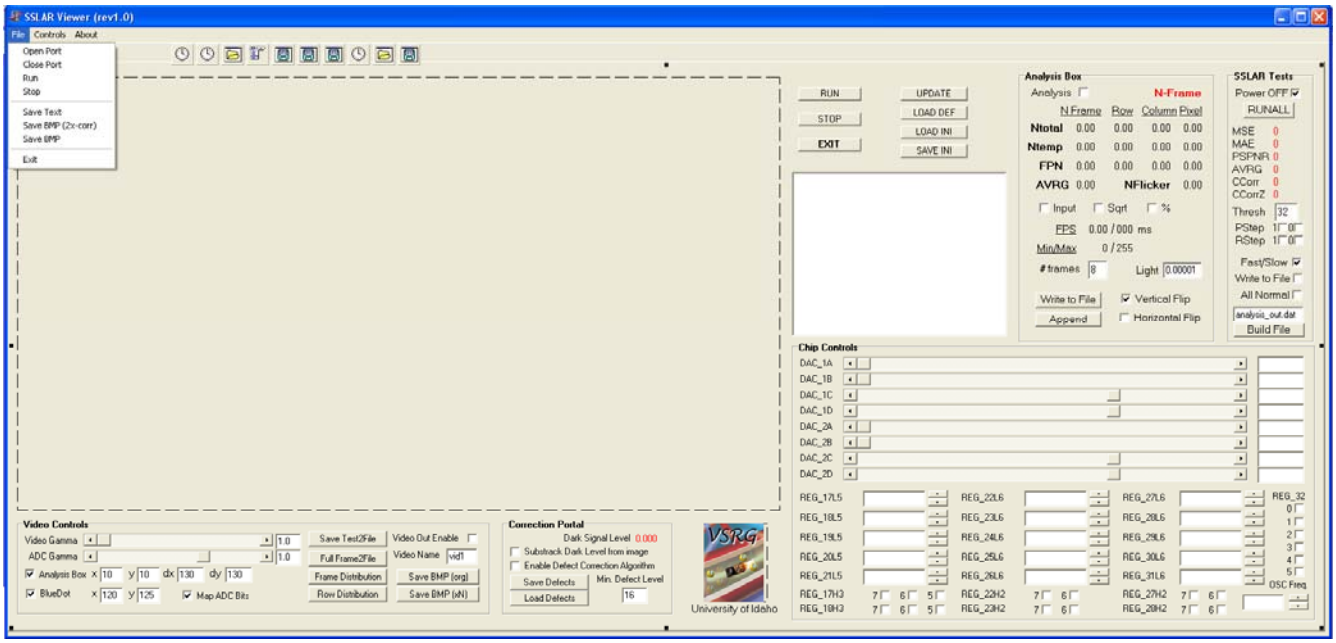


Figure 16. Demonstration and test software for SSLAR IC.

D. Conclusion and Discussions

The 12-bit SSLAR technology in a 720p HDTV format which has 945,744 pixels was sent for fabrication in May 11, 2012 after a delay during tapeout. The delay on the fabrication resulted in 2 months shift on our testing timeline. As a result the testing will be completed in August 2012 after the project period ends in June 30th. Testing will not requiring any cost due to the fact that all required test fixtures, software, and equipment made ready before the project period ends. PI will spend his personal time to complete the task.

Comparing with our previous deign which had 10-bit SSLAR ADC and 30,000 pixels, this new design 30 times larger in terms of pixel count and posses 4 times better ADC bit resolution.

Two undergraduate students were hired during the project. One was a Computer Engineering senior hired for integrated circuit (IC) design tasks and the other one was a Computer Science senior hired for software design tasks. This project not only provided training for these students but also provide platform for them to work on real product grade IC design and testing. Both students graduated in May 2012. They received several job offered and started working right after graduation.

Despite scheduling road blocks, all project goals meet with the exception of testing which will be done after design is received in August 2012.