COVER SHEET FOR GRANT PROPOSALS

State Board of Education

SBOE PROPOSAL NUMBER: (to be assigned by SBOE)	AMOUNT REQUESTED: $50,000
TITLE OF PROPOSED PROJECT: SAVE: Self-organizing Air VEnt System	
SPECIFIC PROJECT FOCUS: Affordable and Smart Home Ventilation System: Automatic zone-to-zone temperature distribution	
PROJECT START DATE: 7/1/13	PROJECT END DATE: 6/30/14
NAME OF INSTITUTION: Boise State University	DEPARTMENT: Office of Sponsored Programs
ADDRESS: 1910 University Dr., Boise, ID 83725	
E-MAIL ADDRESS: osp@boisestate.edu	PHONE NUMBER: (208) 426-4420

	NAME:	TITLE:	SIGNATURE:
PROJECT DIRECTOR/PRINCIPAL INVESTIGATOR	Dr. Gang-Ryung Uh	Associate Professor	Not required
CO-PRINCIPAL INVESTIGATOR			

NAME OF PARTNERING COMPANY: Kinetic Engineering Group	COMPANY REPRESENTATIVE NAME: Nate Calvin

NAME: Nate Calvin SIGNATURE:

Authorized Organizational Representative		
	~~Karen Henry~~ Lisa Jordan, CRA	

SUMMARY PROPOSAL BUDGET

Name of Institution: Boise State University

Name of Project Director: Dr. Gang-Ryung Uh

A. PERSONNEL COST (Faculty, Staff, Visiting Professors, Post-Doctoral Associates, Graduate/Undergraduate Students, Other)

Name/ Title	Salary/Rate of Pay	Fringe	Dollar Amount Requested
Dr. Gang-Ryung Uh, Associate Professor	1 month $88,754/year	32% of salary	$13,018
Graduate Research Assistant (4); to be hired	3 summer months or $6,000/year each @ $2,000/mo	10% of salary (summer rate)	$26,400

% OF TOTAL BUDGET:	79%	SUBTOTAL:	$39,418

B. EQUIPMENT: (List each item with a cost in excess of $1000.00.)

Item/Description	Dollar Amount Requested
SUBTOTAL:	$0

G. TRAVEL:

Dates of Travel (from/to)	No. of Persons	Total Days	Transportation	Lodging	Per Diem	Dollar Amount Requested
Travel to 2 HVAC/Ventilation trade shows. Dates to be determined.	2	3	$300/each	$300/each	$150/per diem	$3,000
					SUBTOTAL:	$3,000

H. Participant Support Costs:

	Dollar Amount Requested
1. Stipends	
4. Other	

I. Other Direct Costs:	Dollar Amount Requested
1. Materials and Supplies Materials for prototyping (wires, registers, electrical components)	$7,582
2. Publication Costs/Page Charges	
3. Consultant Services (Include Travel Expenses)	
4. Computer Services	
5. Subcontracts	
6. Other (specify nature & breakdown if over $1000)	
SUBTOTAL:	$7,582
J. Total Costs: (Add subtotals, sections A through I) **TOTAL:**	$50,000
K. Amount Requested: **TOTAL:**	$50,000
Project Director's Signature: Not required	Date:

INSTITUTIONAL AND OTHER SECTOR SUPPORT

(add additional pages as necessary)

A. INSTITUTIONAL / OTHER SECTOR DOLLARS

Source / Description	Amount
Academic year support for the 4 GRAs working on the project. They will work as both Teaching Assistants and Research Assistants.	$96,000
Summer support for the 4 GRAs working on the project. They will work as both Teaching Assistants and Research Assistants.	$5,000

B. FACULTY / STAFF POSITIONS

Description

C. CAPITAL EQUIPMENT

Description

D. FACILITIES & INSTRUMENTATION (Description)

SAVE: Self-organizing Air VEnt System

1. Boise State University.
2. Principal Investigator (PI): Gang-Ryung Uh
3. This draft is original and was not submitted to any prior HERC RFPs

4. Executive Summary:

U.S. households rely primarily on electricity and natural gas for heating, ventilation, and air conditioning (HVAC). Even though the efficiency of the HAVC has improved over time, the Department of Energy (DOE) reports that air-conditioning and space heating are still responsible for the greatest share of each household utility bill. The DOE strongly recommends U.S. households to install central programmable thermostats that can save around 10% a year on cooling and heating bills by simply turning the thermostat back 7^{o} -$10^{o}F$ for eight hours a day from its normal setting.

Figure 1: The NEST Thermostat Controller

A prime example of the programmable thermostats is the NEST product shown in Figure 1. Nevertheless, a critical drawback of these programmable thermostats is that they can only accurately control the temperature for a localized zone, and zone-to-zone temperatures can vary significantly. For instance, in a room/space that is poorly insulated, this programmable thermostat can make the room/space *too cold* (over-

cooling) or *too hot* (over-heating), which often results in an unexpected increase in the utility bills. Thus, the objective of the proposed ***S**elf-organizing **A**ir **VE**nt* (***SAVE***) system is to solve this critical drawback associated with the current programmable thermostats.

5. Project Objective and Total Amount Requested

To address the aforementioned over-cooling and over-heating problem, multi-zone HVAC systems have been used. The multi-zone HVAC system is part of the initial HVAC installation and consists of one or more central cooling/heating units, individual zone thermostats, a ductwork system, and dampers for controlling airflow to each zone as well as a central controller. These types of systems are exemplified by the *Lennox* HVAC Zone Control products. The over-cooling and over-heating problem can be mostly resolved since each zone is controlled by its own programmable thermostat. Yet, these systems require extremely high initial installation costs and expensive retro-fits in cases where a single zone system is converted into multi-zone systems (i.e. well beyond $10,000).

The advent of inexpensive low-power microprocessors and cheap IR sensors has led to the introduction of programmable battery powered air vent registers. Each battery-powered vent register can be programmed by its own programmable thermostat or from its IR remote temperature controller, which opens or closes the vent to regulate conditioned air according to a programmed setting. A prime example of these types is the *Activent* Vent-Miser ($20 per unit). Though, the disadvantages of the *Activent* products are threefold. First, the existing vent registers need to be removed and replaced by the *Activent* registers. Second, the *Activent* product does not come with any

central controller, and therefore, it can greatly damage a HVAC when all the vent registers happen to be closed while the HVAC unit is operating. Hence, the *Activent* manual strongly warns and recommends a limit of only one-third of the existing vents be replaced with their products. Finally, an individual within a household is required to program each Vent-Miser thermostat to avoid over-cooling and over-heating, which not only makes it difficult for the individual but also makes the programming more prone to errors (you can reword this but I think it's can be quite difficult to be correct.

The ***objective*** of the proposed ***SAVE*** is to address the problem of over-cooling and over-heating via zone-to-zone automatic temperature distribution mechanism. The ***SAVE*** system will achieve a similar outcome of the *Lennox* types of multi-zone HVAC systems with a surprisingly affordable *Activent* Vent-Miser price. The following are notable features of the **SAVE** system compared to *Lennox* and *Activent* products.

- It does not require a retrofit of an existing HVAC system.
- It does not replace any existing vent registers.
- It does not require any stressful programming of zone controllers or air vent registers. Instead, it dynamically finds ideal vent controls that maintain zone-to-zone even temperature distributions throughout an entire house.
- It is safe to use and will not damage the HVAC unit.
- It is fault-tolerant; it can still operate even if one or more vent registers malfunction.
- It is extremely easy to maintain.

For this **SAVE** project, we are requesting ***$50,000,*** which covers four CS and ECE graduate research assistants summer assistantships, one month of PI Uh's summer

salary, electronic parts and materials to build **SAVE** controllers, and travel costs to introduce the **SAVE** system during the annual HVAC trade show.

6. Resource Commitments that Reflect Boise State's Priorities

Since 2005, the University has dedicated resources to the Office of Campus Sustainability led by Dr. John Gardner. In 2010, Boise State became the leading institution in the new Energy Efficiency Research Initiative at Center for Advanced Energy Studies (CAES). The mission of the new Initiative is to increase education and research in energy efficiency, which represents the ultimate objective of the **SAVE** System.

7. The SAVE System's Potential Impact to the Economy of Idaho

There are several significant ways in which SAVE will positively affect the economy of Idaho. First, the ***SAVE*** system can be supported by the State Legislatures for energy efficiency, and it can be supported by Idaho local utility companies as a consumer commodity for the same reason. Second, as long as the ***SAVE*** system implementation, testing and market acceptance look promising, it can easily augment various HVAC products from the *Nest*, *Lennox*, *Activent* and other suppliers, which will help U.S households save cooling and heating bills. By approaching existing manufacturers with enhanced and working versions of their own products by the ***SAVE*** system, we can make it easy for them to visualize the ***SAVE*** system's Intellectual Properties (IPs) in their product line. Third, a provisional patent for the ***SAVE*** system also gives us and Boise State University a sellable piece of IP.

8. The Market Opportunity for the *SAVE* Project

I. *SAVE* System Architecture

Automatic zone-to-zone temperature distribution

The battery powered ***SAVE*** system consists of (1) multiple Zone Controllers (ZCs) (Figure 2.a) and (2) one or more registers (Figures 2.b and 2.c) which are wirelessly paired to each ZC (Figure 2.d). The ZC does not operate a HVAC; instead, it continuously repeats the following tasks while the HVAC unit is operating:

- Measuring the current zone temperature
- Wirelessly receiving temperature information from other ZCs
- Controlling the valves of the wirelessly paired ***SAVE*** registers

Figure 2.a
SAVE **Zone Controller (ZC)**

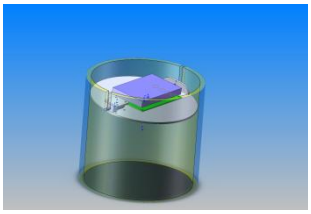

Figure 2.b
SAVE **Register Prototype**

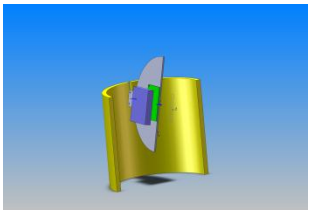

Figure 2.c
Cross-section: ***SAVE*** **Register Prototype**

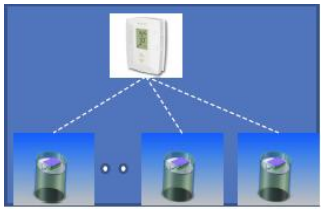

Figure 2.d
SAVE **Zone Controller and wirelessly paired Registers**

The wireless communication for the ***SAVE*** will be done using a low-power RFM12B (433Mhz) radio technology. The radio waves on 433Mhz frequency band, compared to 2GHz microwaves, travel significantly longer, penetrate walls, and leave much better at the same transmission power. Therefore, desired zone-to-zone communication among ZCs can be facilitated for the house size up to 4,000 square feet with RFM12B radio modules without any extra antenna or repeater.

II. How *SAVE* System works

Automatic zone-to-zone temperature distribution

Suppose a house with the proposed ***SAVE*** system, which is configured with three ZCs and each ZC, is paired with two registers as shown in Figure 3.

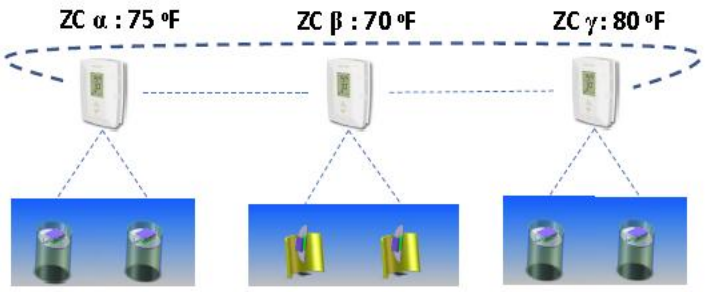

Figure 3. A House with ***SAVE*** : Three Zone Controllers (ZCs) α, β and γ

Additionally assume that the sampled temperatures for ZCs α, β and γ at time t_0 were 75 F, 70 F, and 80 F respectively when the central programmable thermostat turned on air conditioning with 72 F. There are many possible algorithms for automatic controls to achieve an even zone-to-zone temperature distribution. For this project, we will start with a simple algorithm. At any given point of time, the ZC which has the largest delta from the 72 F, opens the valves of its paired registers and all the other registers close their valves. Figure 4 shows the dynamics of the zone-to-zone temperature changes until 72 F.

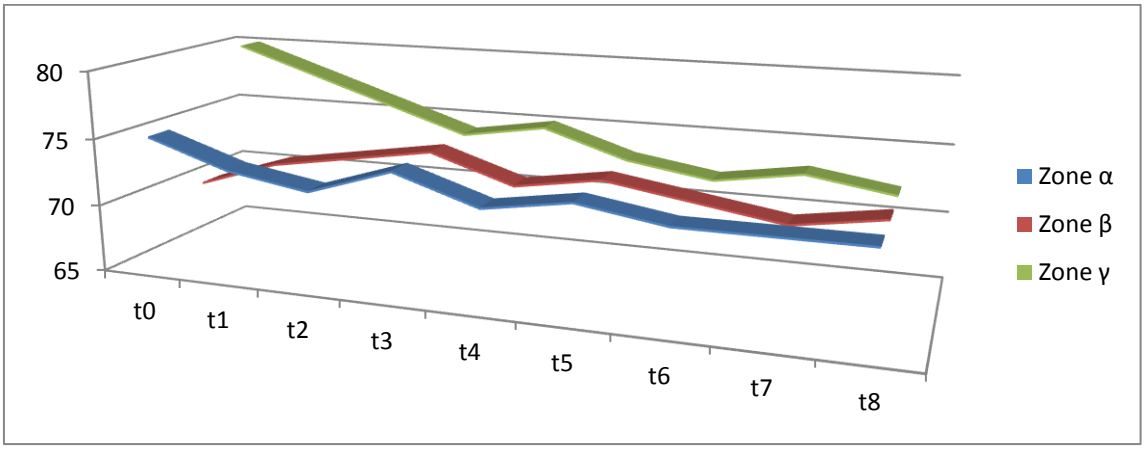

Figure 4. Zone-to-zone automatic temperature distribution with ***SAVE***

III. Where *SAVE* registers will be placed

Automatic zone-to-zone temperature distribution

The ***SAVE*** registers will be installed below existing air vent registers not to interfere with any existing vent fixtures. For easy installation and maintenance (i.e., annual or bi-annual battery replacement), the ***SAVE*** registers (Figure 5.b) will be designed with an expandable rubber insulator to fit securely in either the air duct interface (highlighted in **RED** in Figure 5.a) or the air vent register interface (highlighted in **BLUE** in Figure 5.a.). With this register placement, the ***SAVE*** can be exempt from many mandatory testing required by the Consumer Product Safety Improvement Act.

Figure 5.a.
Air Duct Tubing (Red) and Air Vent Register Interface (Blue)

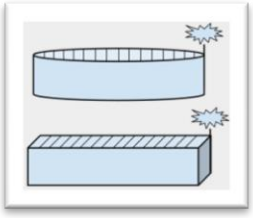

Figure 5.b.
Two types of *SAVE* registers for Air Duct and Air Vent Register Interfaces

IV. Why *SAVE* System is Safe?

Automatic zone-to-zone temperature distribution

Each ***SAVE*** Register is equipped with both temperature and pressure sensors to detect airflow and temperature from an air duct. Each ZC will be able to detect the state of its paired ***SAVE*** Registers, i.e. open, close, or not responding. Each ZC also will be able to detect the health of all the other ZCs and will help prevent the catastrophic case, "*all registers happen to be closed while the HVAC unit is operating*!"

V. Responses to items a), b) and c): *Please refer to Sections 5 and 7.*

9. The Technology and Path to Commercialization

I. *What stage in the process **SAVE** project is currently at*

- January 2013: Kyle Schwab (ECE/CS graduate student) and PI Uh submitted Creation of Works Disclosure to Boise State University and Industry Ventures.
- February 2013: The University and Industry Ventures at Boise State University assigned the ***SAVE*** project Boise State File #130.
- Since January 2013: With the CS Department Support (Dr. Harold Blackman) and PI Uh's research grants, Kyle Schwab and PI Uh have been building required electronic components for ***SAVE*** Zone Controller (ZC) and Registers.
- March 2013: Jared Law (CS graduate student) and Nathan Riskey (CS graduate student) joined the ***SAVE*** project as graduate research assistants.
- March 2013: Nate Calvin, the head of ***Kinetic Engineering Group*** (http://www.kineticengineeringgroup.com/index.html) joined the ***SAVE*** project as a business partner and he is currently building the mechanical prototypes for ***SAVE*** Registers.
- April 2013: A patent agent examined the ***SAVE*** invention in prior art. He summarized three points of novelty and un-obviousness seen in the **SAVE** according to the Title 35 of the United States Code (numbers 101, 102 and 103).
- May 2013: Gregory Cook (CS graduate student) joined the ***SAVE*** project as a graduate research assistant.

II. *What this funding will accomplish*

- Support the research team to build hardware/software and build a deployable SAVE system for testing and benchmarking.
- Support the research team to develop ***SAVE*** ZC and Register with minimal cost.
- Support the research team to meet HVAC manufacturers

III. *What tasks are required to move the **SAVE** project to the next stage and the intended outcome*

- Task: Filing provisional patent for ***SAVE*** project.
- Task: Testing and benchmarking
- Task: Timing of action - Market strategy and planning

  PI Uh submitted a proposal on a ***Flexible Smart System for Lighting*** (**FSS4L**) to HERC-2012, which was not selected for funding. Recently, we found that the LED investment company at the Silicon Valley successfully raised its funding $1.4M with the similar project and technology which we already have. http://www.kickstarter.com/projects/limemouse/lifx-the-light-bulb-reinvented
- Task: Manufacturing plan
- Intended Outcomes: (1) **completion of the provisional patent filing** on the ***SAVE*** system invention and (2) **production of *SAVE* systems that can be deployable at my neighbor's houses.**

10. Commercialization Partners

Nate Calvin, the president of ***Kinetic Engineering Group*** (http://www.kineticengineeringgroup.com/index.html) will be the ***SAVE*** system's commercialization partner. In particular, Nate Calvin and his engineering team will build the mechanical prototypes of the ***SAVE*** system and help us commercialize the SAVE system as a consumer product.

11. Specific Project Plan and Detailed Use of Funds

For the tasks in Table 1, PI Uh will lead the research team of four graduate CS/ECE students – Kyle Schwab, Jared Law, Nathan Riskey and Gregory Cook. All the ***SAVE***

team members have prior industry and academic experience in design and implementation of embedded systems. First, the research team will prepare the electronic and mechanical prototypes for the ***SAVE*** system described above by the 2nd quarter of the project, and we will deploy the prototypes to the houses of the project participants and do the testing and benchmarking the effectiveness of the system during the 3rd and 4th quarters. In addition, PI Uh will prepare the required document for provisional patent filing with the Boise State University. During the 4th quarter, we will begin public ***SAVE*** system demonstrations.

Tasks	1st quarter 7/1/13-9/30/13	2nd quarter 10/1/13-12/31/14	3rd quarter 1/1/14-3/31/14	4th quarter 4/1/14-6/30/14
Electronic prototype				
firmware development				
mechanical prototype				
testing and benchmarking				
patent preparation & filing				
project demonstration				
HVAC trade show				

Table 1. *SAVE* Project Plan

The requested ***$50,000*** will be used to support (1) four CS and ECE graduate research assistants summer assistantships, (2) one month of PI Uh's summer salary, (3) electronic parts and materials, and (4) travel costs to introduce the **SAVE** system during the annual HVAC trade show.

12. Institutional and Other Sector Support

Computer Science Department and PI Uh at Boise State University will support the participating graduate students for the ***SAVE*** project by providing research assistantships during the 2014 academic year.

FACILITIES, EQUIPMENT & OTHER RESOURCES

FACILITIES: Identify the facilities to be used at each performance site listed and, as appropriate, indicate their capacities, pertinent capabilities, relative proximity, and extent of availability to the project. Use "Other" to describe the facilities at any other performance sites listed and at sites for field studies. Use additional pages as necessary.

Laboratory: Micron Engineering Center 302 - Computer Science Research Lab

Clinical:

Animal:

Computer: PI Uh has one 24-core Intel Xeon CPU (2.4Ghz) server and two Core I7 servers to manage the project development source code and report the progress of the proposed SAVE development. Two Windows 7 workstations and two Linux workstations for firware development.

Office: Micron Engineering Center 302-N

Other: PI Uh has two floating licenses of IAR WorkBench to develop firmware on Atmel 8-bit microcontrollers

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MAJOR EQUIPMENT: List the most important items available for this project and, as appropriate, identifying the location and pertinent capabilities of each.

20 Atmel XMEGA-B1 XPLAINED Evaluation Kits, 8 Atmel JTAGICE3, 5 BeagleBoardXM, 1 Pandaboard, and 3 Raspberry pi

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OTHER RESOURCES: Provide any information describing the other resources available for the project. Identify support services such as consultant, secretarial, machine shop, and electronics shop, and the extent to which they will be available for the project. Include an explanation of any consortium/contractual arrangements with other organizations.

Geared motors and drivers, temperature/pressure sensors, acceRFM12B (433Mhz) radio modules, acclerometers, Atmel Raven, and TI CC2530 ZigBee network processor development kits

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Biographical Sketch of Gang-Ryung Uh

Associate Professor of Computer Science — U.S. resident
Dept. of Computer Science
Boise State University
1910 University Drive, Boise ID 83725 — uh@cs.boisestate.edu
http://cs.boisestate.edu/~ uh — Tel: (208) 426-5691

Professional Preparation

B.A.	1987	Economics *Hankuk University of Foreign Studies*, Seoul, Korea
M.S.	1992	Computer Science *Florida State University*, Tallahassee, FL
Ph.D.	1997	Computer Science *Florida State University*, Tallahassee, FL

Appointments

08/2008 - present	:	Associate Professor, Dept. of Computer Science, *Boise State University.*
08/2010 - 07/2011	:	Research Associate (sabbatical) for the NSF grant CNS-0964413, *Static Pipelining, an Approach for Ultra-Low Power Embedded Processors* Dept. of Computer Science, *Florida State University*, Tallahassee, FL.
08/2002 - 07/2008	:	Assistant Professor, Dept. of Computer Science, *Boise State University.*
06/2007 - 12/2007	:	On-line Race Detection Tool Developer (Intel Contract), *Intel Performance, Analysis and Threading Lab*, Champaign, IL.
05/2005 - 08/2005	:	Research Associate, School of Electrical Engineering, *Seoul National University*, Seoul, Korea.
01/1998 - 07/2002	:	Embedded System Tools Developer, *Lucent Technologies*, Allentown, PA.

Five most relevant publications (student author names shown in italic font)

- *I. Finlayson*, *B. Davis*, *P. Gavin*, **G. Uh**, D. Whalley and G. Tyson, "Improving Processor Efficiency by Statically Pipelining Instructions," *ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems (LCTES)*, June 2013, Seattle, WA.
- *I. Finlayson*, **G. Uh**, D. Whalley and G. Tyson, "An Overview of Static Pipelining," *IEEE Computer Architecture Letters (CAL)*, ISSN:1556-6056, vol. 11, no. 1, January 2012, selected as the BEST paper and presented at the 19th IEEE International Symposium on HPCA, Feb 2013, Shenzhen, China.
- **G. Uh**, R. Cohn, B. Yadavalli, R. Peri and and *R. Ayyagari*, "Analyzing Dynamic Binary Instrumentation Overhead," *Workshop on Binary Instrumentation and Application*, October 2007, San Jose, CA.
- *M. Yang*, **G. Uh** and D. Whalley, "Efficient and Effective Branch Reordering Using Profile Data," *ACM Transactions on Programming Languages and Systems (TOPLAS)*, vol. 26, no. 6, pp 667–697, 2002.

- *M. Yang*, **G. Uh** and D. Whalley, "Improving Performance by Branch Reordering," *Proc. of ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 1998, Montreal, Canada.

Complete listing of current support

PI	Google Faculty Research Award	$37,400
Co-PI	Korea Evaluation Institute of Technology (KEIT) Grant NO. 10041725	$154,289
Co-PI	Small Medium Business Administration (SMBA) Grant NO. 0004537	$130,594

Synergistic Activities

- **2012 Google Faculty Research Award - Open-Source ARM Cortex A8 Compiler:** An optimizing ARM Cortex A8 compiler development via streamlining LLVM and VPO compilers to generate high performing ARM Cortex A8 machine code, which can match the performance of Cortex A9 with significantly reduced power consumption.

- **Ad-hoc Wireless Physical System Development:** (1) Zigbee-based Wireless ad-hoc LED (Light Emitting Diode) network that can be accessed and controlled using smart phones and (2) Four-wheel Lego Mars Rover that can be wirelessly controlled over Bluetooth.

- **Pin-based Dynamic Cache Simulator Development for Shared Address Space (SAS) Multiprocessor Architectures:** On-line PIN cache simulation tool that reports cache performance for x86 multi-threaded applications with various cache coherence strategies, i.e., MSI, Dragon, and Directory-based.

- **LejOS Robotics Activities Development for Undergraduates and High School students:** (1) Intiation of Computer Science Robotics Club (2009) and (2) creation of Robotics activities during e-Day (K12 under-represented students) and e-Girls (9th–10th grade female students) to broaden under-represented students' participation into STEM.

- **Conference:** (1) Programming Committee members for INTERACT-15 and INTERACT-16, (2) Local chair ACM SIGPLAN Conference on Languages, and Compilers and Tools for Embedded Systems (LCTES 2005), and (3) Programming Committee members for ICPP'03, and LCTES'02–LCTES'05.

Collaborators & Other Affiliations

- **Collaborators:** Dan Connors (Colorado State University); Gary Tyson (Florida State University); Jae Ryu (University of Idaho); Robert Cohn (Intel); Ramesh Peri (Intel); Santosh Pande (Georgia Institute of Technology); Zhenghao Zhao (Florida State University).

- **Graduate Advisors:** David Whalley (Florda State University); Theodore Baker (Florida State University).

- **Thesis Advisor and Postgraduate-Scholar Sponsor:** Christopher Healy (Furman University); Frank Mueller (North Carolina State University); Prasad Kulkarni(University of Kansas); Steve Hines (Google);

GANG-RYUNG UH, Ph.D. – CURRICULUM VITAE

A Contact Information

Department of Computer Science, Boise State University,
1910 University Drive, Boise, Idaho 83725
E-mail: uh@cs.boisestate.edu,
Home page: http://cs.boisestate.edu/∼uh,
Phone: 208.426.5691

B Research and Teaching Interests

Optimizing Compilers, Computer Architecture, Dynamic Performance Evaluation, and Embedded Systems.

C Formal Higher Education

1997	Ph.D	Major: Computer Science. Florida State University, Tallahassee, Florida. Dissertation: *"Effectively Exploiting Indirect Jumps"*
1993	M.S.	Major: Computer Science. Florida State University, Tallahassee, Florida. Thesis: *"Predicting Consumer Expenditure Behavior with Neural Nets"*
1987	B.A.	Major: Economics. Hankuk University of Foreign Studies, Korea.

D Professional Employment

2008 – present	Associate Professor, Computer Science Department, Boise State University.
2010– 2011	Research Associate (sabbatical) for the NSF grant CNS-0964413, *Static Pipelining, an Apporach for Ultra-low Power Embedded Processors*, Dept. of Computer Science, Florida State University, Tallahassee, FL.
2002 – 2008	Assistant Professor, Computer Science Department, Boise State University.
2007 (Jun–December)	Consultant, Intel Performance, Analysis and Threading Lab, Champaign, USA.
2006 (May–August)	Consultant, Intel System Software Lab, Hillsboro, USA.
2005 (Dec)	Research Faculty, Seoul National University, Korea.
2005 (May–August)	Research Faculty, Seoul National University, Korea.
2000 – 2002	Research Scientist, Agere Systems, USA.
1998 – 2000	Research Scientist, Lucent Technology, USA.
1990 – 1997	Research/Teaching Assistant, Department of Computer Science, Florida State University, USA.

E University Level Teaching

E.1 Courses taught

1. Quantitative Computer Architecture	(grad)	Boise State University, Boise, Idaho
2. Advanced Topics in Compilation	(grad)	Boise State University, Boise, Idaho
3. Introduction to Computer Science I	(undergrad)	Boise State University, Boise, Idaho
4. Introduction to Computer Science II	(undergrad)	Boise State University, Boise, Idaho
5. Embedded Systems Design in C	(grad)	Boise State University, Boise, Idaho
6. Programming Language & Translation	(undergrad)	Boise State University, Boise, Idaho
7. Problem Solving in C	(undergrad)	Florida State University, Tallahassee, Florida

E.2 Courses created

1. Quantitative Computer Architecture	(grad)	Boise State University, Boise, Idaho
2. Advanced Topics in Compilation	(grad)	Boise State University, Boise, Idaho
3. Embedded Systems Design in C	(grad)	Boise State University, Boise, Idaho
4. Problem Solving in C	(undergrad)	Florida State University, Tallahassee, Florida

E.3 Courses revised in large

1. Introduction to Computer Science I	(undergrad)	Boise State University, Boise, Idaho
2. Introduction to Computer Science II	(undergrad)	Boise State University, Boise, Idaho
3. Programming Language & Translation	(undergrad)	Boise State University, Boise, Idaho

F Publications

F.1 Refereed Journals

1. I. Finlayson, **Gang-Ryung Uh**, D. Whalley and G. Tyson. *"An Overview of Static Pipelining,"* IEEE Computer Architecture Letter (CAL), ISSN:1556-6056, Volume 11, No. 1, Jan 2012. The paper was selected as the BEST paper and presented during the 19th IEEE International Symposium on HPCA.

2. **Gang-Ryung Uh**, Yuhong Wang, David Whalley, and et al. *"Compiler Transformations for Effectively Exploiting a Zero Overhead Loop Buffer,"* In the journal of Software Practice & Experience, Volume 35, pages 393-412, 2005.

3. W. Kreahling, D. Whalley, M. Bailey, X. Yuan, **Gang-Ryung Uh**, R. Van. *"Branch Elimination via Multi-Variable Condition Merging,"* In the journal of Software Practice & Experience, Volume 35, pages 51-74, 2005.

4. Jinhwan Kim, Yunheung Paek, **Gang-Ryung Uh**. *"Code Optimization for a VLIW-style network processing unit,"* In the journal of Software Practice & Experience, Volume 34, pages 847-874, 2004.

5. Minghui Yang, **Gang-Ryung Uh**, David Whalley. *"Efficient and Effective Branch Reordering Using Profile Data,"* In ACM Transactions on Programming Languages and Systems (TOPLAS),Volume 26, Number 6, pages 667-697, 2002.

6. **Gang-Ryung Uh** and David Whalley. *"Effectively Exploiting Indirect Jumps,"* In the journal of Software Practice & Experience, December 1999, pages 1061-1101.

F.2 Refereed Conferences

1. I. Finlayson, B. Davis, P. Gavin, **Gang-Ryung Uh**, D. Whalley, M. Sjalander and G. Tyson. *"Improving Processor Efficiency by Statically Pipelining Instructions,"* In the proceeding of ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems (LCTES), June 2013, Seattle, WA.

2. Doosan Cho, Ravi Ayyagari, **Gang-Ryung Uh**, and Yunheung Paek. *"Preprocessing Strategy for Effective Modulo Scheduling on Multi-Issue Digital Signal Processors,"* In the Proceedings of the 16th International Conference on Compiler Construction, March, 2007, Braga, Portugal.

3. Wankang Zhao, Prasad Kullkarni, David Whalley, Christopher Healy, Frank Mueller, **Gang-Ryung Uh**. *"Tuning WCET of Embedded System,"* In the Proceedings of IEEE 10^{th} Real-Time and Embedded Technology and Applications Symposium, May 2004, Toronto, Canada.

4. W. Kreahling, D. Whalley, M. Bailey, X. Yuan, **Gang-Ryung Uh**, R. Van. *"Branch Elimination via Multi-Variable Condition Merging,"* In the Proceedings of European Conference on Parallel and Distributed Computing (EuroPar03), August 26-29, 2003, Klagenfurt, Austria.

5. J. Kim, S. Jung, Y. Paek, and **Gang-Ryung Uh**. *"Experience with a Retargetable Compiler for a Commercial Network Processor,"* In the Proceedings of the 2002 International Conference on Compilers, Architecture and Synthesis for Embedded Systems, 2002, Grenoble, France.

6. **Gang-Ryung Uh**, Yuhong Wang, David Whalley, and et al. *"Techniques for Effectively Exploiting a Zero Overhead Loop Buffer,"* In the Proceedings of the 9th International Conference on Compiler Construction (CC'2000), pages 157-172, March 2000, Berlin, Germany.

7. Minghui Yang, **Gang-Ryung Uh**, David Whalley. *"Improving Performance by Branch Reordering,"* In the Proceedings of ACM SIGPLAN Conference on Programming Language Design and Implementation, pages 130-141, June 1998, Montreal, Canada.

8. **Gang-Ryung Uh**, David Whalley. *"Coalescing Conditional Branches into Efficient Indirect Jumps,"* In the proceedings of International Static Analysis Symposium, pages 315-329, September 1997, Paris, France.

9. **Gang-Ryung Uh**, Daniel Schwartz. *Predicting Consumer Expenditure Behavior with Neural Nets,"* In the Proceedings of IEEE'93 World Congress on Neural Networks.

F.3 Refereed Workshops

1. I. Finlayson, **Gang-Ryung Uh**, D. Whalley and G. Tyson. *"Improving Low Power Processor Efficiency with Static Pipelining,"* In the proceeding of 15th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), Feburary, 2011, San Antonio, TX.

2. **Gang-Ryung Uh**, Robert Cohn, Bharadwaj Yadavalli, Ramesh Peri, and Ravi Ayyagari. *"Analyzing Dynamic Binary Instrumentation Overhead,"* In the Proceedings of the Workshop on Binary Instrumentation and Applications, October, 2006, San Jose, USA: **appeared in the ACM SIGARCH Computer Architecture News, ISSN:0163-5964.**

3. Doosan Cho, Ravi Ayyagari, **Gang-Ryung Uh**, and Yunheung Paek. *"Instruction Re-selection for Iterative Modulo Scheduling on High Performance Multi-issue DSPs,"* In the Proceeding of the 1^st International Workshop on Embedded Software Optimization, August, 2006, Seoul, Korea: **published in Lecture Notes in Computer Science (LNCS), ISSN:0302-9743.**

4. **Gang-Ryung Uh**. *"Tailoring Software Pipelining for Effective Exploitation of Zero Overhead Loop Buffer,"* In the Proceedings of the 7^{th} International Workshop on Software and Compilers for Embedded Systems (SCOPES 2003), September 24-26, 2003, Vienna, Austria: **published in Lecture Notes in Computer Science (LNCS), ISSN:0302-9743.**

5. **Gang-Ryung Uh**, Yuhong Wang, David Whalley, and et al. *"Effective Exploitation of a Zero Overhead Loop Buffer,"* In the Proceedings of ACM SIGPLAN Workshop on Languages, Compilers, and Tools for Embedded Systems, pages 10-19, May 1999, Atlanta, USA: **published in ACM SIGPLAN Notices, Volume 34, Issue 7, ISBN:1-58113-136-4.**

F.4 Patent

1. **Gang-Ryung Uh**, Doosan Cho, and et. al. *"Effective Modulo Scheduling for Multi-issue High Performance Digital Signal Processor"* is filed January 2006.

2. **Gang-Ryung Uh**, David Whalley, and et. al. *"Compiler Optimization for Exploiting Zero Overhead Loop Mechanism"*, Inventor Number: 2083757, Patent Number:6367071, Approval Date: April 2, 2002.

G Invited Talks/Presentations

1. *"Improving Processor Efficiency by Statically Pipelining Instructions',"* KOCSEA Technical Symposium, Atlanta, Georgia, 2012.

2. *"LLVM-VPO Compiler Infrastructure for a Low Power Embedded Processor,"* Seoul National University, Seoul, Korea, 2012.

3. *"Overview of Statically Pipelined Processor,"* ETRI, DaeChun Korea, 2012.

4. *"Compiler Optimization Strategies for Mobile Processors,"* ETRI and Monuel ELFWAND Project Workshop, DaeChun, Korea, 2012.

5. *"Architecture and Compiler Techniques to Improve Processor Energy Efficiency,"* Samsung System-On-Chip (SOC), Seoul, Korea, 2012.

6. *"PIN - Dynamic Binary Instrumentation,"*, NASA Advanced Supercomputing Division, Ames, CA, USA, 2006.

7. *"StarCore VLES SC1400 DSP and Compiler Optimization,"* Samsung Electronics, Seoul, Korea, 2005.

8. *"Effective Modulo Scheduling for VLES SC1400 DSP,"* Seoul National University, Seoul, Korea, 2005.

9. *"Compiler Optimization Strategy to Reduce Power without Degrading Performance,"* NASA Advanced Supercomputing Division, NASA Ames, CA, USA, 2004.

10. *"Compiler Optimization Strategy to Reduce Power without Degrading Performance"*, Agere Systems, Allentown, PA, USA, 2004.

11. *"Tailoring Software Pipelining for Effective Exploitation of Zero Overhead loop buffer,"* SCOPES, Vienne, Austria, 2003.

H Funding

1. Principle Investigator, Google Faculty Research Award, *"Preprocessing for Modulo Scheduling within Open-Source ARM Cortex-A8 Compiler,"* $37,400, August 2012 –.

2. Co-Principle Investigator, Korea Evaluation Institute of Industry Technology (KEIT), Grant NO.10041725, *"ELFWAND: Building the Service and Software Foundation for Personalized Smart Device Sensor Applications,"* $154,289 (for Boise State University), Jun 2012 – May 2015.

3. Co-Principle Investigator, Korea Small Medium Busines Adiministration, Grant NO. 0004537, *"Development of Virtual Machine for Smart Sensor Network Access Control-based Platform,"* $130,594 (for Boise State University), Jun 2011 – May 2013.

4. Principle Investigator, NASA Idaho EPSCoR, *"PIN Based Non-Uniform Memory Access (NUMA) Memory Simulator,"* $30,000, May 2009 – August 2010.

5. Principle Investigator, INTEL Corporation, *"Multi-threaded PIN Simulator Desgin,"* $25,000, Jan 2007–Oct 2011.

6. Principle Investigator, NASA Idaho EPSCoR, *"Compiler Optimization for Ultra-Low Power Wireless Sensor Signal Processor,"* $8,000, Nov 2005–Nov 2006.

7. Principle Investigator, Brain Pool (Korean Federation of Science and Technology Societies) *"Compiler Infrastructure Development,"* $20,000, *Period*: May 2005–Dec 2005.

8. Principle Investigator, NASA Idaho EPSCoR, *"Optimizing Compiler Benchmark Infrastructures for Ultra-low Power Embedded Processors,"* $60,294.00, *Period*: Oct 2003–Aug 2004.

9. Principle Investigator, NSF Idaho EPSCoR, *"Instruction Selection Sensitive Software Pipelining for Effectively Exploiting Zero Overhead Loop Buffer,"* $50,800, Mar 2003–Dec 2003.

10. Principle Investigator, Dean's Office, *"Automatic Code Generator for Embedded Processors,"* $30,000, Jan 2003–.

H.1 Equipments awarded

1. INTEL Corporation, 2x Intel Itanium IA64 MP 1.3Ghz Rackmount server, $11,655.00, Mar 2007.
2. INTEL Corporation, 4x Intel Xeon MP 2.7Ghz Rackmount Server, $28,159.00, Oct 2006.
3. AGERE SYSTEMS Corporation, DSP16000 software tools and DSP16410 development boards, $36,000.00, Dec 2005.
4. CYPRESS SEMICONDUCTOR Corporation, PSoC development kits, $10,000.00, Oct 2005.

I Mentoring

I.1 Graduate Students

- MS student: Kyle Schwab: *SAVE: Self Organizing VEnt Control*.
- MS student: Jared Law: *SAVE: Self Organizing VEnt Control*.
- MS student: Nathan Riskey: *SAVE: Self Organizing VEnt Control*.
- MS student: Gregory Cook: *SAVE: Self Organizing VEnt Control*.
- Ph.D committee: Doosan Cho, Dept of ECE, Seoul National University.
- MS Chair: Jaremy Creechley, Topic: *LAZYCAT: A Lazy XMLPL Compiler and Runtime System*, October 2012.
- MS student: Pallayya Sarma Karra, Tentative topic: *Visualization of Dynamic Loop Profiling Information*.
- MS committee: Kevin Nuss, Topic: *A Tool to Aid in the Parallelization of C and Fortran Programs*.
- MS Chair: Ravi Ayyagari, Topic: *A Dynamic Loop Profiling, Optimization and Detection Tool*, August 2007.
- MS Chair: Arpita Ghosh, Topic: *Retargeting MPEG Decoder to Digital Signal Processor*, May 2007.
- MS committee: ChokSheak Lau, Georgia Institute of Technology, Topic: *An Optimization Framework for Embedded Processors with Auto-Modify Addressing Modes*, Nov 2004.

I.2 Undergraduate Students

- Ryan Baird (CS), Topic: *LLVM-VPO Compiler for ARM Cortex A8*
- Jason Wall (CS), Topic: *3D NBody Gravitational Simulation*
- Mark Stewart (CS), Topic: *3D NBody Gravitational Simulation*
- Paul Turner (Physics), Topic: *3D NBody Gravitational Simulation*
- Dan Crow (CS), Topic: *Visual Interactive Assembly Level Optimizer for DSP16000*, August 2005

- Steve Mathie (CS), Topic: *Visual Interactive Assembly Level Optimizer for DSP16000*, August 2005
- David Zuercher (CS), Topic: *Automatic Code Generator for Embedded Processors*, Dec 2004
- Charles Paulson (CS), Topic: *Automatic Code Generator for Embedded Processors*, April 2004

J Professional Service

2010-2011	Program Committee Member, Workshop on Interaction between Compilers and Computer Architectures (INTERACT)
2004–	Chair of Board of Directors, Idaho Korean Community Association
2002–	Reviewer of numerous journal and conference articles, approx. 40.
2005	Local Chair, ACM SIGPLAN/SIGBED 2005 Conference on Languages, Compiles, and Tools for Embedded Systems (LCTES).
2005	Session Chair, ACM SIGPLAN/SIGBED 2005 Conference on Languages, Compiles, and Tools for Embedded Systems (LCTES).
2003	Student Poster Session Chair, ACM SIGPLAN/SIGBED 2005 Conference on Languages, Compiles, and Tools for Embedded Systems (LCTES).
2003	Program Committee Member, ACM SIGPLAN/SIGBED 2005 Conference on Languages, Compiles, and Tools for Embedded Systems (LCTES).
2003	Program Committee Member, International Conference on Parallel Processing (ICPP).
2002	Program Committee Member, ACM SIGPLAN/SIGBED 2005 Conference on Languages, Compiles, and Tools for Embedded Systems (LCTES). Tenure period.

K References

References available upon request.

KINETIC
ENGINEERING GROUP

May 10, 2013

Boise State University
Attn: Dr. Gang-Ryung Uh

Dear Dr. Uh,

We are writing to express our support for your proposal for funding under the HERC Idaho Incubation Fund program towards developing **Self-Organizing VEnt (*SAVE*)** System.

The purpose of your proposed scope of work is important to the industry and we are interested in research and development opportunities that will assist in moving this technology to a stage that can be commercially marketed.

Kinetic Engineering Group is comprised of a team of forward-thinking, degreed engineers focused on bringing innovative projects and designs to market. Although the majority of our prior projects involve the process of development starting from the 'ground up'; we have also successfully improved several existing processes and products using the same approach. In particular, we will provide the expertise, technology and experience is researching and designing the mechanical components of the ***SAVE*** Registers that best suits the intended market and meets the performance expectations. We have over 40+ yrs of manufacturing and design of electrical/mechanical components, which provided the basis for bridging the gap between R&D and full-scale manufacturing. We are prepared to provide the following support towards the SAVE project. Specific experience/expertise include:

1) Full Mechanical Design of components;
    a. Simulation of System (FEA, CFD and Dynamic Motion Studies);
    b. DFC/DFM criteria;
    c. Life Test Analysis (simulated and empirically tested);
    d. Prototype and model verification;
    e. Beta Test Articles/Case-study implementation;
2) Electrical PCA Design:
    a. CM selection;
    b. DFM/DFC;
    c. PSpice Analysis;
3) Business Model Development
    a. Production Tooling/Options/Selection;
    b. NRE Identification;
    c. Cost Projections;
    d. Business Model Development

We are committed to providing industry with the most current technology and see the opportunity to partner with Dr. Uh's research at Boise State University to be extremely valuable.

Kinetic Engineering Group looks forward to our involvement and potential for interaction leading to the development and commercialization of Dr. Uh's ***SAVE*** system as a consumer product.

Best regards,

Nate Calvin

Digitally signed by Nate Calvin
DN: cn=Nate Calvin, o=AeroLEDs, ou=CEO/President, email=Nate@AeroLEDs.com, c=US
Date: 2013.05.14 21:51:12 -06'00'

Nate Calvin (Nate@kineticengineeringgroup.com)

Kinetic Engineering Group