ARC: Automata processor for Research Computing

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Institution: Boise State University

Summary of project accomplishments for the reporting period

During this reporting period we were able to evaluate the performance characteristics of key components of the ARC system, procure, install and provision the server for general use by members of the CS department at Boise State University. The proposed server was also fitted with a K20 NVIDIA GPU (at additional expense by the department) to allow us to compare GPU + Direct I/O in conjunction with a CPU, Automata Processor and/or both of processor types. As the automata processor chip is undergoing a redesign the actual hardware component will be delivered in the fall of 2015. As of now we are working with a hardware emulator, provided by Micron, to conduct research in the application areas of biological sequence analysis and graph isomorphism. A joint project with Dr. Kaylanaraman from WSU Pullman has started and we have been working together over the course of this summer. We intend to publish our results in fall and apply for NSF MRI funding in December 2015.

Summary of budget expenditures for the period just completed

Following hardware procurements were made during this period:

1. R430 Server from Dell, Inc.
2. A PCIe-SSD from Fusion IO
3. 2nd Generation PCI boards with Automata processor from Micron, Inc – to be delivered in Fall 2015.

Demonstration of economic development/impact, including the following as applicable:

- Patents, copyrights, Plant Variety Protection Certificates received or pending

None

- Technology licenses signed, start-up businesses created, and industry involvement

None

- Private sector engagement

We have been working with Terry Leslie from Micron Technology for evaluating the Automata Processors application in Read-detection in proteins and Graph Isomorphism in social networks. This is work in progress and will continue to be investigated by PI's research group. Mikel Joaristi, a newly recruited graduate student will be starting a MS this fall and will use the procured

Automata processor machine to develop machine-learning algorithms suited for the Non-Von-neumann architecture.

- Jobs created

None

- External funding

None

- Any other pertinent information

None

Numbers of faculty and student participation as a result of funding

Three faculty – two PI's and Dr. Ananth Kalyanaraman from UW were involved in the research and procurement related to the Automata Processor. As we received the funding late in the spring of 2015 best suited students had signed up for internship elsewhere. We were however able to find a graduate student who will continue to use the hardware starting fall of 2015.

Description of future plans for project continuation or expansion

As the automata processor is undergoing a redesign the actual hardware component will be delivered in the fall of 2015. As of now we are working with a hardware emulator to conduct research in the application area of biological sequence analysis and graph isomorphism. Our plan is to continue using emulation kit for prototyping the systems and work towards the publications in IPDPS and SIGMOD. As these applications are novel uses of the architecture, our work will identify performance bottlenecks to inform design of future generation of automata processor.

Expenditure Report

$50,948.34 expensed $40.66 remaining 99%.

Commercialization revenue

None

Additional metrics established specific to this individual project

Our goal to create a unique hardware resource for the researchers in the university has been met. We now have a substantial research instrument to help accelerate applications that effectively exploit the NFA representation of state space. In collaboration with our research partner we have identified two application areas and have been using the emulation software to evaluate our results. The problem of graph isomorphism is of huge importance and the PI's current graduate student Akshay Kansal (also a Micron employee) has been working over the last 9 months on ways to scale clique queries on evolving graphs. As a part of his thesis, he will be also porting the implementation of these algorithms to Automata Processor (AP) architecture. In addition, a second student Mikel Joaristi will be investigating the use of AP architecture

for developing machine learned models and explore possible applications in training Neural nets. Although, the AP hardware will be available in fall, we stand better prepared to use the hardware when it arrives. The acquisition of the resource has fostered cross-institutional collaboration.