PROPOSAL NUMBER: (to be assigned by HERC after submission)		**TOTAL AMOUNT REQUESTED:** $152,600	
Proposal Track (select one): Proof of Concept			
NSF I-Corps participation: **Have you participated in, or plan to participate in the NSF I-Corps Program?** I have not participated yet, but I am registered. **If so, when did you or will you?** I am registered in I-Corps Aspire #8 (March–April 2026)			
TITLE OF PROPOSED PROJECT:		Design of a low-cost optical wavelength division multiplexing transceiver in CMOS	
SPECIFIC PROJECT FOCUS:		Microelectronics/Semiconductors	
PROJECT START DATE: September 1, 2026		**PROJECT END DATE:** August 31, 2027	
NAME OF INSTITUTION: Boise State University		**DEPARTMENT:** Electrical and Computer Engineering	
ADDRESS: 1910 University Dr., Boise, ID, 83725-2075			
E-MAIL ADDRESS: osp@boisestate.edu		**PHONE NUMBER:** (208)-426-4420	
PROJECT DIRECTOR/ PRINCIPAL INVESTIGATOR	**NAME:**	**TITLE:**	**SIGNATURE:**
	Alexander Sheldon	Assistant Professor	
NAME OF PARTNERING COMPANY: American Semiconductor		**COMPANY REPRESENTATIVE NAME:** Doug Hackler, CEO	
SIGNATURE: 			
Authorized Organizational Representative	**NAME:** Ella Christiansen	**SIGNATURE:** 	

PRIMARY IDAHO PUBLIC INSTITUTION	Boise State University
PROJECT TITLE	Design of a Low-Cost Optical Wavelength Division Multiplexing Transceiver in CMOS
PRINCIPAL INVESTIGATOR	Dr. Alex Sheldon, Assistant Professor, Boise State University
KEY PERSONNEL	• Doug Hackler, CEO, American Semiconductor • Kjersti Martino, Director of Product Management, Inneos • Two Boise State graduate student research assistants
TOTAL AMOUNT REQUESTED	$152,600

SIGNIFICANCE OF PROJECT AND PROJECT OBJECTIVES

In this collaboration between a university and private sector partner, we are pursuing IGEM HERC proof-of-concept track funding to develop a low-cost fully-integrated optical-to-electrical and electrical-to-optical transceiver for future use in high-speed Ethernet adapters and/or smart network interface cards (collectively referred to as NICs) [2]. This optical transceiver will enable future NICs to **transfer data faster**, at a **lower cost,** and at a **lower power consumption per bit transferred**, which will ultimately **enable higher computation speeds** in data centers, as these speeds are currently limited by the speed that data can be moved between processing units (xPUs); Central Processing Units (CPUs), Graphics Processing Units (GPUs), Neural Processing Units (NPUs), Tensor Processing Units (TPUs), etc. Further, developing this technology can increase Idaho's economic competitiveness in a market that is potentially worth **billions**. This project aligns with the request for proposals in the microelectronics/semiconductor funding priority area, and in turn with the 2023–27 Idaho Higher Education Research Strategic Plan. It also has an impact to the artificial intelligence priority. The technology can be used to enable growth in artificial intelligence by improving data throughput while reducing cost and power consumption.

SIGNIFICANCE

The Problem. The recent resurgence of generative artificial intelligence (genAI) and large language models (LLMs), has led to an exponential increase in the need for internet bandwidth globally, as represented by internet traffic. See **Figure 1**. In turn, we have reached an ever-expanding bottleneck in every segment of the internet backbone; IC-to-IC, rack-to-rack, and data-center-to-client [1].

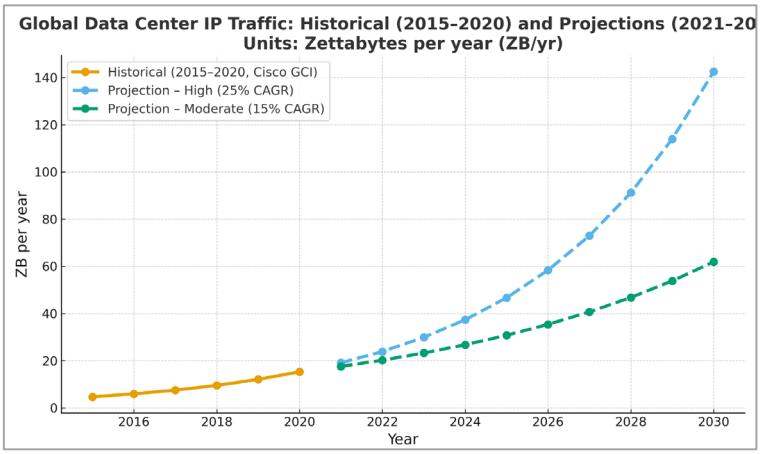

Fig. 1: Data Center Internet Protocol (IP) Traffic Projections

Challenges & Opportunities. The resulting bottleneck has led to a significant growth in the market for NICs [2]. Currently, the cost of a single long-range 800GbE transceiver, which is used in data-center-to-client, is about $3k [4] due to the high cost of assembly and alignment of the typical multi-IC solution and/or plug-in optics [5]. Fabricators typically implement high-speed optical transceivers like those used in NICs using a multi-IC solution with one electrical integrated circuit (IC), one photonic IC, and a separate vertical-cavity surface-emitting laser (VCSEL) [5]. However, this method is expensive both to fabricate and assemble, due to the need for exotic semiconductor materials, such as indium phosphate (InP), and gallium nitride (GaN), for the

photonic IC, and the requirement for micrometer-precision alignment of components. In this proposal, I aim to remove the photonic IC and use self-aligning processes as used in IC packaging/assembly to reduce NIC costs. This leads to two fundamental hypotheses that must be tested to successfully implement the proposed solution: 1) electronic and photonic circuits can be implement on the same bulk CMOS IC, and 2) IC-to-IC bonding can be done cost-effectively while allowing for automatic optical alignment of the laser while still allowing for efficient cooling of the lasers. These two hypotheses are critical as the proposed solution relies on them to meet benefits as detailed in the rest of the proposal.

Our Solution & Expertise. To meet the opportunity, our team will develop a novel solution to reduce the cost of NICs **by a factor of ten**. To reach this potentially transformative outcome, we will implement the optical/photonic components directly on a low-cost (in volume) bulk CMOS integrated circuit (IC) (the predominant technology used to commercially manufacture ICs) rather than the traditional, and more expensive, photonic integrated circuit. We will conduct this study to prove two novel hypotheses, that we can: (1) integrate a hybrid photonic/electronic integrated circuit in a bulk CMOS process, and (2) develop a bonding process that allows for automatic optical alignment of a laser, and for cooling of the VCSEL. Hypothesis (1) will provide a path to including both electronic and photonic components in the same IC without significantly increasing cost, therefore optimizations can be made at the system level, where the optimum choice can be made for each component to be implemented as an electronic and/or photonic circuit. Hypothesis (2) will provide a solution, in Idaho, to enable the development of heterogeneous integration of multiple different processes beyond this project.

Our team has the necessary partners in place to complete this work. As a new assistant professor at Boise State University (started in January 2026) with nearly nine years of academic and industrial experience in the design of high-speed analog integrated circuits, I am well positioned to lead an effort as principal investigator (PI), and will guide student researchers along with local and national industry partners in the development of this technology. I completed the conceptual design of the proposed optical transceiver while I was a member of Dr. Mohamed Elamien's research group at McMaster University in Hamilton, Ontario, Canada. Currently no intellectual property has been developed but any developments throughout the design process will need to be evaluated for ownership based on who has contributed to the invention. This conversation has been started with Boise State University technology transfer office. American Semiconductor in Boise, Idaho will provide fabrication for a robust IC-on-IC assembly process, and Inneos in Pleasanton, California is providing the VCSELs to drive the optical fiber.

Global Market & Potential Benefits for Idaho. The United States market for NICs is predicted to reach $16 billion by 2028 [2]. Additionally, there is a predicted $1.7 trillion in global spend in data center infrastructure (including information technology (IT) hardware) over the next five years [3]. Due to this exponential market growth, it is an **opportune time for the government and industry in Idaho** to invest in this area, and in the personnel needed to develop technologies to fill this market gap. Investment in the proposed project will result in the development of intellectual property and manufacturing capability that will enable Idaho to compete in this growing market.

PROJECT OBJECTIVES

We will complete six project objectives to produce the prototype transceiver:

1. **Model Target Device**—Establish device features based on current literature and measurements.
2. **Develop System-level Design**—Determine component/circuit level specifications from device model.
3. **Design Photonic Components**—Design photonic components and manufacturing recipe.
4. **Complete Circuit Design**—Boise State team completes design work and sends IC for fabrication at Taiwan Semiconductor Manufacturing Company (TSMC).
5. **Package Circuit with Laser**—American Semiconductor fabricates substrate and combines with IC from TSMC and VCSEL from Inneos.
6. **Validate System Performance**—Boise State team rigorously verifies prototype performance.

Specific Project Plan and Timeline

In a 1-year project planned from September 1, 2026–August 31 2027, the project team will develop a proof-of-concept optical wavelength division multiplexing wireline transceiver for use in NICs. Assuming a successful outcome, we estimate that we could convert the proof of concept into a profitable business in about 3–5 years after the project ends (see Future Funding section for more detail).

Technology Readiness Level & Project Scope

Here are details about our current and targeted technology readiness level, and how we have scoped the project design to provide robust and meaningful deliverables within a one-year timeframe.

Technology Readiness Level. The project goal is to bring the proposed hybrid electrical/photonic IC transceiver technology from technology readiness level (TRL) 2 to TRL 4, and the packaging process to TRL 6. See **Figure 2**. As our partnership serves to illustrate, we believe there is a high potential for near-term transfer to the private sector. TRL 2 indicates that the technology concept is formalized, TRL 4 that we have validated the technology in lab, and TRL 6 that we have demonstrated the technology in a relevant environment.

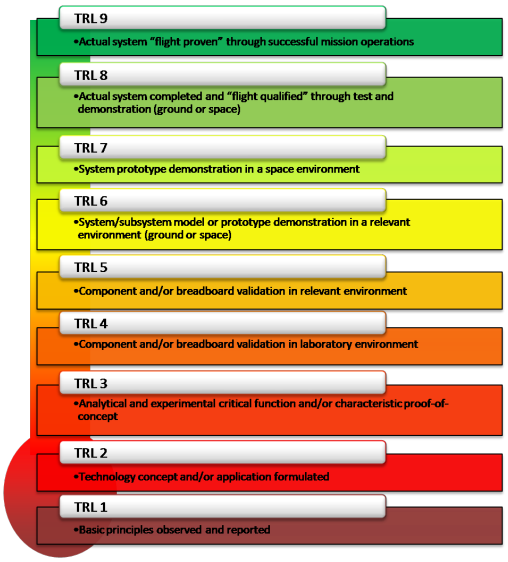

Fig. 2: Technology Readiness Levels

The ability to bring the packaging process to TRL 6 is due to American Semiconductor, given their extensive experience in the area. They would be the ideal supplier to package parts in a future commercial product.

Setting a One-Year Project Scope. Since we want to quickly prove the concept during the one-year development time this grant would fund, we will develop a 2x25 Gb/s PAM-4 optical transceiver in a 65-nm CMOS process. This prototype limits the scope of a potential 800GBASE NIC [4] product as much as possible to allow for quick development, as typically a project of this scale would require a large team of engineers two full-time years to successfully develop. To this end, this IC will implement two 25Gbps (reduced from the four 100Gbps in an 800GBASE NIC [4]) serial links each operating on a different optical wavelength over a single fiber (reduced from two fibers in an 800GBASE NIC [4]) with optical multiplexing/de-multiplexing, which is an extension to work from Ives et al. [7]. We will implement the analog and photonic portion of the serial link, and will convert the optical signal to/from eight 3.125Gbps serial electrical signals (i.e. no physical layer (PHY) implemented).

Taking these steps results in a feasible project that we can complete with two full-time PhD students. Each will work 20-hours per week during the academic term, and 40-hours per week during the summer. One will focus on high-speed serial links, and the other on photonic integrated circuits. Both students and I will work with Doug Hackler at American Semiconductor to characterize their current IC-to-IC assembly process and determine requirements, and any adaptations for the proposed project.

Objective 1: Model Target Device (pre-award, Summer 2026)

We will begin by developing models based on literature, and device measurements we make, of sample components. This will be completed prior to award receipt as it contributes to, and enables, other aspects of my research program. The electronic components have fully-validated models from TSMC, so here we will focus on the optical and electro-optical components, in particular the photodiode and VCSEL.

The photodiodes we will implement in the CMOS IC are critical in converting the optical signal from the optical fiber to an electrical signal that we can then further process electronically. We will use Synopsys Sentaurus technology computer-aided-design (TCAD) software to simulate the photodiodes and

determine the optimum design for this application. Boise State participates in the Synopsys University program, so already has access to this software.

The VCSELs, from Inneos, convert the electrical signal to an optical power. This optical power is transferred across the optical fiber. We have received preliminary data from Inneos but to fully characterize the VCSELs we will need to measure the device samples at various bias points and temperatures. These measurements can be completed with a vector network analyzer (VNA) at Boise State. After measurements the data can be fitted to a physics-based model from the literature [6].

OBJECTIVE 2: DEVELOP SYSTEM-LEVEL DESIGN (PRE-AWARD, SUMMER 2026)

I have begun the system-level design, and will finish over the summer after we complete the device models from objective 1. This system-level design will result in component specifications that we will need to use in the circuit-level designs in objective 3 and 4.

The architecture of the NIC will be a direct-drive optical transceiver where the CMOS circuit directly modulates each of the VCSELs. See **Figure 3**. In each of the NICs the light from two VCSELs is multiplexed onto the fiber to double the data rate of the NIC. Additionally, the received light is demultiplexed into the two different wavelengths and processed by separate electrical receivers.

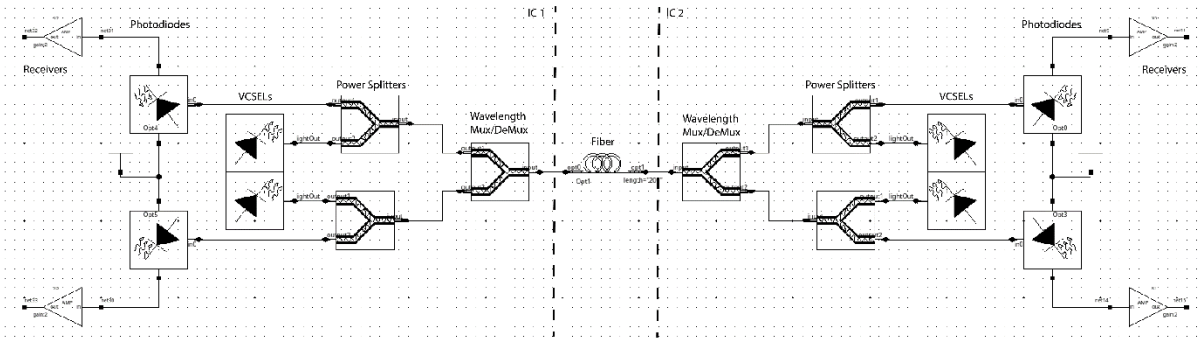

Fig. 3: Simplified System-Level Block Diagram

OBJECTIVE 3: DESIGN PHOTONIC COMPONENTS (SEPTEMBER TO OCTOBER 2026)

Once we have attended to the preliminaries in objectives 1 and 2, we can begin work on the heart of the project. First, the student researcher focused on photonic integrated circuits will use Cadence Virtuoso and Ansys Lumerical software to adapt waveguides from Ives, Sarkar and Hajimiri studies [7] into the TSMC 65nm process design kit (PDK). We selected this technology to balance cost with potential high-speed performance. Once we can provide a thorough study of the waveguide geometry and recipe for manufacture, we will we create models for use in the circuit simulation in objective 4. The photonic circuit design is relatively simple as the technique of implementing the photonic components is not a very stable process so, we want to keep the risk to the minimum to allow for testing of the process.

The photonic components that are required to implement this design are edge couplers to connect the fiber into the IC, wavelength division multiplexer/de-multiplexer to combine and separate the two different wavelengths of light, power splitter/combiner, and couplers to connect to the VCSELs and photodiodes.

OBJECTIVE 4: COMPLETE CIRCUIT DESIGN (SEPTEMBER 2026 TO MARCH 2027, SUBMIT FOR MANUFACTURE IN MID-MARCH 2027)

While one student researcher completes objective 3, the second, with a focus on high-speed serial links, will begin work in parallel on the circuit design of components that do not directly depend on the waveguide components. In November when the bulk of objective 3 is complete both students will work together to design the high-speed data path based on my system-level design. This objective will be the major focus of the project as it aligns most with my expertise and has the most potential for innovation.

From an initial literature review the main innovation in the electronics will be in the low-noise receiver, in particular the transimpedance amplifier at the input. Other circuit components that will be required are a

continuous-time linear equalizer to compensate for the fiber and waveguide loss, a high-speed digital equalizer (feed-forward or decision-feedback equalizer), a VCSEL driver to control the current of the VCSEL, and a serializer-deserializer (SerDes) to split the serial data path into multiple lower speed data streams to be transferred out of the IC. Additionally design-for-test (DfT) circuitry will be implemented to ease validation.

Objective 5: Package Circuit with Laser (April to June 2027)

We will deliver the ICs to American Semiconductor, and personnel will package it with the VCSEL. Their expertise in complex packaging will enable us to develop a system solution that will achieve the stated performance at a low cost. The IC will be flip-chip mounted on a flexible substrate. The VCSELs will be mounted on the other side of the substrate with holes for the light to enter the IC. The optical fiber will be edge coupled to the IC. For this prototype the electrical inputs and outputs will be routed to a connector for test.

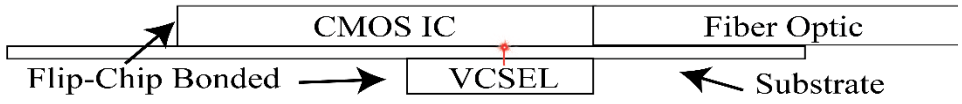

Fig 4: Diagram of Packaged System

Objective 6: Validate System Performance (July to August 2027)

Once American Semiconductor delivers the packaged ICs back to the Boise State research team, we will rigorously validate prototype performance. Validation of the prototype system will be completed by connecting two of the prototypes to a field-programmable gate array (FPGA) board with high-speed transceivers with an optical fiber connected between the ICs and random data will be transmitted back and forth to measure the bit-error rate (BER); the number of failed bits over the total number of transferred bits. Assuming the system works as expected, validation is time-consuming (due to the amount of data that needs to be transferred, and the number of configurations) but relatively simple. The difficulty arises if it does not immediately work as expected. In this situation a high-speed oscilloscope will be used in conjunction with test circuitry implemented on the IC to debug.

Potential Economic Impact

We believe project outcomes, a relatively short path to production at scale, and an expanding global market promise real economic impacts for Idaho. Again, assuming a successful outcome, we estimate that we could convert the proof of concept into a profitable business in about 3–5 years after the project ends. Here are two possible paths that affect potential impacts.

- **Develop an Idaho Start-up**—Ideally, a motivated graduate student will be involved in this part of the project and will want to take the product to market in Idaho either as a startup, or in partnership with an existing Idaho company. This would lead to job creation and economic growth for Idahoans.
- **Work with Existing Companies**—Alternatively, if we find a large company such as Cisco that is already in this market, we could license the intellectual property to them to use in their future products. Another option is to find a smaller company that wants to enter this market, such as Inneos.

We will design and fabricate the IC at the core of the prototype NIC in TSMC 65-nm bulk CMOS. This is a low-cost (in volume) process, with an estimated 12-inch wafer cost of $5.6k [8] and an estimated IC size of 3mm x 3mm for a proposed four wavelength 400Gbps transceiver IC. Our team estimates that we can fabricate about 6,700 of these ICs per wafer, leading to a unit cost of about $0.84. In addition, to the per-IC cost, the mask set cost for these ICs in production is about $620k [9]. Pessimistically, we would need to make two all-layer revisions in production, leading to a non-recoverable cost of $1.86 million. This can be amortized over three years of sales with an intended volume of one million parts per year.

For IC packaging, we estimate a cost of $1000 per wafer. Overall, this would result in a per-IC cost of $1.61. The potential product would require two ICs, eight VCSELs from Inneos ($24 each in low quantity, large quantity price is to be negotiated), and board assembly and packaging ($25 per board at

moderate quantity). Therefore, assuming a gross margin of 58%, this results in a sales price of $350 which is a **factor of ten** below current sales prices of equivalent products despite the very pessimistic cost estimates based on low quantity quotations.

The direct impact to Idaho of this project is difficult to predict accurately but, some potential details will be discussed here. At a minimum this project will contribute to two new highly-qualified individuals with PhDs in a growing area of industry that local companies will have the opportunity to attract. Also, this project will contribute to the creation of valuable academic-industry connections that I will continue to develop through my research at Boise State enabling many more opportunities to bring federal research dollars to Idaho. In the best-case scenario, this research would lead to multiple patents which can be developed into an Idaho-based startup operating in a billion-dollar industry. This would further lead to much more economic development in Idaho in the form of tax dollars and dozens of well-paying jobs.

Criteria for Measuring Success

We have two sets of criteria for measuring success as we complete the specifics of the project, and also as we consider potential future economic impact.

Project Criteria

Table 1: Criteria by objective

#	OBJECTIVE	COMPLETED WHEN…
1	Model Target Device	VCSEL and photodiode models can be simulated in Cadence Virtuoso & Ansys Lumerical.
2	Develop System-level Design	The link budget analysis shows that communication is possible, and we have tables of required specifications for components.
3	Design Photonic Components	Multiplexer/De-multiplexer layout is complete and simulations show results that agree with system-level design, or differences are understood and can be compensated elsewhere.
4	Complete Circuit Design	Circuit-level simulations agree with system-level design, or differences are understood and compensated elsewhere. Then design files are sent to TSMC for manufacture.
5	Package Circuit with Laser	Samples are received from American Semiconductor to validate.
6	Validate System Performance	Measured performance matches system-level simulations, or differences are understood and design revisions are made to correct for a future revision.

Criteria to Assess Economic Potential

Participation in I-Corps Aspire will help in the assessment of any potential economic impact. Throughout my participation in the program, I will need to complete market research, including customer interviews, this will allow us to quantify the expected impact. At a minimum progress will be presented to the HERC board through the semi-annual reporting process during the project and then yearly thereafter. Any additional information on the market that is gathered during I-Corps will be used to adapt and optimize the scope of the work. If any material changes to the scope and/or budget as described in this proposal are expected these will be reported to the HERC board before any changes are made.

The economic potential will be evaluated on a monthly basis throughout the project based on customer interviews. This assessment will be done by evaluating the potential revenue of such a product as well as the number of jobs that would be created in Idaho. In addition to any potential revenue, any possibility for intellectual property protection, including patents, will be pursued when it makes competitive and/or economic sense. The value of any intellectual property will be estimated before application, with

assistance from the Boise State technology transfer office, to make a quantitative decision on the financial benefits of the resulting intellectual property.

Anticipated Development Challenges/Barriers

Due to the complexity of this project, there is potential for challenges that could risk failure of the project. In this section, I will discuss some of the challenges that we can foresee and our risk management plan for both these foreseen challenges and any additional unforeseen challenges.

Schedule risk. Since the design work is complex and difficult to accurately predict, we have reduced the scope of the design as much as possible while still testing the core hypotheses. In my experience the design should be doable in the given schedule but, if delays occur, the scope will be re-evaluated continuously to ensure that value is still produced. A go/no-go decision will be made before ICs are submitted for fabrication in March. The decision will be made based on if the current design can successfully test the two hypotheses with greater than 80% probability. If a no-go decision is made an analysis of the impact will made. Two possible fabrication runs are indicated in the schedule in Appendix A (03/11 and 04/22) which can lead to completion of the project within the year. If a delay is great enough to miss the 04/22 deadline the HERC board will be consulted with an impact analysis.

Budget risk. There are two main areas where budget changes could be possible. First, IC fabrication, if the area required to fabricate changes substantially this would change the cost to fabricate, all attempts will be made to stay within the estimated $3mm^2$. Second, packaging, since the cost of packaging depends on many parameters determined in the design there could be errors in the cost estimates. Added costs are very unlikely to be over ten percent of the budget however, all changes that will impact the budget will be communicated to the HERC board with an impact analysis.

Disproven hypothesis. There is a risk that either of the two hypotheses will be disproven. Based on the experience of the PI, and a thorough literature review this is not expected. If this is the case investigation into alternative methods, to meet the goals of the project, will be made, and a plan for how to proceed with the most value generated will be created. This plan would be presented to the HERC board as it would mean a substantial change to the project scope.

Budget

Refer to the budget spreadsheet for the detailed budget.

Budget Justification

The requested budget is $152,600. The 1-year project will commence from Sept. 1, 2026–Aug. 31, 2027.

Table 2: Summary of budget justification by line item.

LINE-ITEM REQUEST	JUSTIFICATION	TOTAL REQUEST
Personnel (salary and fringe)	1.5-months of PI summer salary, two full-time graduate research assistants at 20 hours per week during the academic term, 40 hours per week during the summer.	$86,100 ($78,900 salary + $7,200 fringe)
Equipment	Required equipment is already available at Boise State University and American Semiconductors.	$0
Travel	Since industry partner is local no travel is necessary.	$0
Participant Support	None.	$0
Other Direct Costs	Student tuition and health insurance, materials, and IC fabrication and packaging.	$66,500
		$152,600

A. PERSONNEL

Dr. Sheldon is the Principal Investigator (PI) and is not requesting any academic year salary. The salary cost for the PI is calculated using his institutional base salary rate. Dr. Sheldon has committed one-and-a-half summer months for this project. The PI will be responsible for system-level design of the prototype as well as mentoring and managing students throughout the design process including, but not limited to, determining circuit-level specifications required for student designs, conducting design reviews at regular intervals in the circuit design process, and ensuring robust circuit design techniques are implemented. The total salary request for the PI is $18,900.

Salary for the two full-time graduate student research assistants is requested at a rate of $30,000 per year per student. Both students will work on this project full time, 20 hours per week during the academic year and 40 hours per week during the summer. The total salary request for students is $60,000.

Fringe benefits for the PI (20.45%) are salary-based and cover retirement contribution, health, dental, life insurance, and employment taxes. Fringe rates for students are salary-based (4% for the academic year, 10% for the summer) and cover employment taxes. The total fringe benefit request is $7,200.

The total request for personnel is $86,100 ($78,900 for salary, and $7,200 for fringe).

B. EQUIPMENT

None, all equipment is already acquired or in the process of being acquired.

C. TRAVEL

None, no travel costs will be required as industry partner is in Boise, ID.

D. PARTICIPANT SUPPORT

No participant support costs are requested.

E. OTHER DIRECT COSTS

Materials and Supplies. To complete the proposed design the computer-aided-design (CAD) software Lumerical, from Ansys, is required. As quoted from Ansys the cost of a single seat is $3,300 which could be shared between myself and the two students.

The company Muse Semi organizes a multi-project wafer submission to cost-effectively manufacture at TSMC for the 65-nm process chosen for this work the costs is $5,800/mm^2 and the expected IC size of the prototype is 3mm^2, resulting in a fabrication cost of $17,400. We will receive one hundred ICs from the MPW submission which will be plenty to fully validated performance. To test the circuit various components will be needed; optical fiber to simulate the channel in the application, connectors to get the electrical signals out of the IC, potting compound to improve cooling, etc. The estimated cost is $500.

In addition to the IC fabrication, there are costs associated with the etching step, required to finish the manufacture of the waveguides on the IC, and with manufacturing the substrate, and packaging the ICs and VCSELs on the substrate. Since the etching process will need to be determined by trial and error and the packaging cost will depend on the actual design of the IC and substrate, we estimate the cost as $12,000 for successfully packaging 3-4 samples. This cost is estimated based on the PIs past experience in the semiconductor industry and communication with American Semiconductor.

Publication Costs. $1,500 for publications; $1,275 repository licensing fee, and $225 for page charges.

Student Costs. Graduate student tuition and health insurance is included as part of their hiring package. Tuition is $12,304.60 per student and health insurance is $3,538.50 per student. Also, there is a library subscription and materials fee of $70 per student Total student costs are $31,800.

G. TOTAL DIRECT COSTS

Total direct cost request is $152,600. No indirect costs are requested.

PROJECT MANAGEMENT

Here are more details about the team composition and our intended communication practices.

PROJECT TEAM

- **Alex Sheldon (PI), Boise State University**—Will use robust academic and industrial experience in designing high-speed analog integrated circuits to lead the project. Will guide students and coordinate all team member activity and communication and information sharing strategies while being attentive to project scope, budget, and schedule.
- **Two PhD Graduate Student Research Assistants, Boise State University**—We will hire student researchers with experience in analog integrated circuit design to start in September 2026. We have completed interviews for these positions and are evaluating the short-listed candidates for admission to the Electrical and Computer Engineering PhD program at Boise State.
- **Doug Hackler, American Semiconductor**—As the chief executive officer of American Semiconductor in Boise, Mr. Hackler has committed to work with the Boise State research group to advance packaging capability towards the low-cost (in volume), and automatically aligned assembly process that would be required to economically manufacture the proposed NICs
- **Kjersti Martino, Inneos**— I have been in contact with Dr. Martino at Inneos in Pleasanton, California who will provide the vertical-cavity surface-emitting lasers (VCSELs) used to drive the optical fiber. Inneos has agreed to provide product samples for the proposed prototype.

COMMUNICATION

Boise State will lead the project with primary communication taking place over email. Since American Semiconductor is located in Boise (15 minutes by car from Boise State) regular onsite meetings will be scheduled during Summer 2027 when packaging will occur. During the entire course of the project, I will hold a weekly status meeting with both students, and Doug and Kjersti included when necessary. Outside of these dedicated meetings I will be available, as required, to support students as this is already part of my role at Boise State University.

PROJECT MANAGEMENT GANTT CHART

Table 3: Project Timeline

Legend: PI (principal investigator), AS (American Semiconductor), S1 (First Graduate Student), S2 (Second Graduate Student)

#	OBJECTIVE	*Sum. 26*	*Sept. 26*	*Oct. 26*	*Nov. 26*	*Dec. 26*	*Jan. 27*	*Feb. 27*	*Mar. 27*	*Apr. 27*	*May 27*	*Jun. 27*	*Jul. 27*	*Aug. 27*
1	Model Target Device	PI												
2	Develop System-level Design	PI												
3	Design Photonic Components		S1	PI+ S1										
4	Complete Circuit Design		S2	S2	S1+ S2	S1+ S2	S1+ S2	S1+ S2	PI+ S1+ S2					
5	Package Circuit with Laser									AS +S1 +S2	AS +S1 +S2	AS +S1 +S2		
6	Validate System Performance												PI+ S1+ S2	PI+ S1+ S2

Additional Institutional and Other Sector Support

Boise State will provide academic year support for the PI, Alex Sheldon. We will use capital equipment that the university either owns, or that we will purchase from other funds outside this potential grant. See details in Appendix A for this equipment.

Future Funding

We will pursue future funding to scale the prototype with our targeted customer in mind. Through my participation in the NSF I-Corps training program, I will develop a strategy to bring the product to market. There are multiple directions this could go based on the type of customer to whom we intend to market the product. Regardless, we could co-develop the intellectual property into a project with further funding coming from small business grants such as the National Science Foundations' (NSF) Small Business Technology Transfer (STTR) program, or Translation to Practice (TTP) program.

Assuming this project is successful this additional funding would be used scale the design to meet the 800GBASE specification including, scaling the transceiver to work at 100Gbps PAM4, and to work with four wavelengths and two fibers. Secondly, work will need to be done to implement the other layers of the network stack to make this a plug-and-play product. Lastly, planning to scale the supply chain is needed, including relationships with TSMC, American Semiconductor, and Inneos will need to be developed to determine costs and potential added value that can be created for customers.

Dissemination of Results

The research described in this proposal is Fundamental Research as described in National Security Decision Directive 189, dated September 21, 1985, and the USD (AT&L) memoranda on Fundamental Research, dated May 24, 2010, and on Contracted Fundamental Research, dated June 26, 2008. As Fundamental Research, the University shall be free to publish or disseminate the results of this research or otherwise treat such results as in the public domain.

References

[1] Cisco Systems, Inc., *Cisco Global Cloud Index: Forecast and Methodology, 2015–2020*, White Paper C11-738085, Nov. 2016. Available: https://www.cisco.com/c/dam/en/us/solutions/collateral/service-provider/global-cloud-index-gci/white-paper-c11-738085.pdf

[2] "Ethernet Adapter and Smart NIC Market to Exceed $16 Billion by 2028," Dell'Oro Group, Redwood City, Calif., Aug. 1 2024. [Online]. Available: https://www.delloro.com/news/ethernet-adapter-and-smart-nic-market-to-exceed-16-billion-by-2028.

[3] E. Kok, J. Rauer, P. Sachdeva, and P. Pikul, "Scaling bigger, faster, cheaper data centers with smarter designs," McKinsey & Company, Aug. 1, 2025. [Online]. Available: https://www.mckinsey.com/industries/private-capital/our-insights/scaling-bigger-faster-cheaper-data-centers-with-smarter-designs.

[4] Arista Networks OSFP-800G-2LR4 Compatible 800GBASE 2 × LR4 OSFP Closed Finned Top PAM4 1310 nm 10 km DOM Dual Duplex LC/UPC SMF Optical Transceiver Module (SKU: 229663)," FS (COM), [Online]. Available: https://www.fs.com/products/229663.html.

[5] J. Robinson *et al*., "FPGA-Programmable 512 Gbps 2.5D DWDM Photonic Network Interface Card," *2024 Conference on Lasers and Electro-Optics (CLEO)*, Charlotte, NC, USA, 2024, pp. 1-2.

[6] K. Kim, J. -S. Kim, J. -Y. Kim and W. -Y. Choi, "A Large-Signal SPICE Model for VCSEL Based on Piece-Wise Linear RLC Elements," in IEEE Photonics Technology Letters, vol. 36, no. 24, pp. 1477-1480, 15 Dec.15, 2024, doi: 10.1109/LPT.2024.3493956.

[7] C. Ives, D. Sarkar and A. Hajimiri, "Subtractive Photonics in Bulk CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 11, pp. 3030-3043, Nov. 2023, doi: 10.1109/JSSC.2023.3308915

[8] "Understanding Wafer Cost," AnySilicon, [Online]. Available: https://anysilicon.com/wafer-cost.

[9] "Semiconductor Wafer Mask Costs," AnySilicon, [Online]. Available: https://anysilicon.com/semiconductor-wafer-mask-costs.

APPENDIX A: FACILITIES AND EQUIPMENT

The research described in this proposal will take place in my lab, the Novel Techniques in On-Chip VLSI & Analog (NOVA) Circuits Lab which is located in the Micron Engineering Center (MEC) in room 409 at Boise State University. In this lab we have adequate space for myself and the two students to complete the design and validation of the prototype. The lab is equipped with general-purpose electronic measurement equipment as part of my start-up package; including a high-speed (1GS/s) oscilloscope, power supplies, multimeters, soldering equipment.

In addition, to the electronic measurement equipment we have access to computer-aided-design servers which are owned by Boise State which will be used for all design work, for this project, by myself and students. The server is equipped with an AMD EPYC 9554 64-Core processor, and 754GB of RAM. Boise State has licenses for Synopsys Sentaurus TCAD, Cadence Virtuoso, and MATLAB for all faculty and students. Additionally, my lab has a single license for Ansys Lumerical, and another will be purchased with the budget from this grant.

There are also two specialty pieces of measurement equipment, as mentioned in the body of this proposal, required for this project; a vector network analyzer (VNA), and a field-programmable gate array (FPGA) board with high-speed electrical transceivers. The VNA is already owned by Boise State, and in the possession of a different lab, this will be borrowed for the preliminary portion of this project. The FPGA board is in the process of being purchased as this enables multiple aspects of my research program.

Also included in this section are quotes and lead time estimates for any material or supply costs over $1,000.

- **Figure 5.** Cost of multi-project wafer run through MuseSemi for the TSMC 65nm process.
- **Figure 6.** Schedule of multi-project wager runs through MuseSemi for the TSMC 65nm process.
- **Figure 7.** Quote from Ansys for Lumerical suite.

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A GSME COMPANY

Services Schedule FAQ University FinFET Program 日本語

TSMC MPW SHARED TAPEOUTS

	180 MS RF G	180 HV BCD ...	65 MS RF GP	65 MS RF LP	28 HPC+ RF
Metal	1p6m_4X1N8KA	1p6m_4X1U40KA	1p9m_6X1Z1U_ALRDL_14.5KA	1p9m_6X1Z1U_ALRDL_14.5KA	1p9m_6X1Z1U_ALRDL_28KA
	1p6m_4X1U40KA				1p10m_5X2Y2R_ALRDL_28KA
Core (V)	1.8	1.8/5	1.0	1.2	0.9
I/O (V)	3.3	70 max	2.5	2.5	1.8
MiM Cap. (fF/um2)	2	2	2	2	Not applicable
MiM Cap. Location	M5-M6	M5-M6	M7-M8	M7-M8	Not applicable
High Resist Poly (K ohm/sq)	1	3	Not applicable	Not applicable	Not applicable
Deep Trench	Not applicable	Not supported	Not applicable	Not applicable	Not applicable
Min. Area (mm2)	5	5	1	1	1
Y Dim. (mm)	40KA: 2, 3, 5	2, 3, 5	1, 2, 3	1, 2, 3	1, 2, 3
	8KA: 3, 5				
X Dim. (mm)	min 0.6, AR <= 3	min 0.6, AR <= 3	min 0.6, AR <= 3	min 0.6, AR <= 3	min 0.6, AR <= 3
Backgrind thickness (mils)	12	12	12	12	12
Cycle Time (days)	42	62	67	67	78
Sample Qty.	40	40	100	100	100
Price ($/mm2)	1,250	1,500	5,800	5,800	13,800

Fig 5: Price for Fabrication at TSMC (from musesemi.com/shared-block-tapeout-pricing)

MUSE SEMICONDUCTOR
A GSME COMPANY

Services Schedule FAQ University FinFET Program 日本語

TSMC MPW SHARED TAPEOUT SCHEDULE

Type to search 65

Tech (nm)	Flavor	Trial	Final	Tapeout	Est. Ship
65	MS RF GP	02/25/2026	03/04/2026	03/11/2026	06/07/2026
65	MS RF LP	04/08/2026	04/15/2026	04/22/2026	07/19/2026
65	MS RF GP	04/29/2026	05/06/2026	05/13/2026	08/09/2026
65	MS RF LP	06/03/2026	06/10/2026	06/17/2026	09/13/2026
65	MS RF GP	07/08/2026	07/15/2026	07/22/2026	10/18/2026
65	MS RF LP	09/02/2026	09/09/2026	09/16/2026	12/13/2026
65	MS RF GP	10/07/2026	10/14/2026	10/21/2026	01/17/2027
65	MS RF LP	11/04/2026	11/11/2026	11/18/2026	02/14/2027
65	MS RF GP	12/02/2026	12/09/2026	12/16/2026	03/14/2027

Fig 6: Schedule for Fabrication at TSMC (from musesemi.com/shared-block-tapeout-schedule)

Ansys part of SYNOPSYS

ANSYS, Inc.
2600 ANSYS Drive
Canonsburg, PA 15317
US

Quotation

Ansys Contact: Catriona Scheffer
catriona.scheffer@ansys.com

Quote #: Q-506306
Date: Jan-29-2026
Expires On: Feb-28-2026

Customer: Boise State University
1910 University Drive
Boise, Idaho 83706
United States
Alex Sheldon
asheldon@boisestate.edu

Ansys Account ID: 1116957

Payment Terms: 30 NET
Billing Frequency: One-time
Payment Term Description: Net payment is due 30 days from invoice date.

Notes for Customer: Purchase Orders MUST reference our Quote Number and the Payment Term listed above

#	Product	AT / APC	QTY	Start Date	End Date	Unit Price ($)	Effective Total ($)
1	Ansys Academic Research Lumerical (1 Task) - Lease	License / LAN, STL, ARL	1	Feb-8-2026	Feb-8-2027	5,680.00	5,680.00

List Total: $ 5,680.00
Total Discount: $ 2,380.00
Net Total: $ 3,300.00

Above Pricing does not include any applicable taxes (Sales, VAT, GST).

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Fig 7: Ansys Lumerical Quotation

Effective 05/20/2024 NSF BIOGRAPHICAL SKETCH OMB-3145-0279

IDENTIFYING INFORMATION:

NAME: Sheldon, Alexander Wayne

ORCID iD: https://orcid.org/0000-0003-4123-0024

POSITION TITLE: Assistant Professor

PRIMARY ORGANIZATION AND LOCATION: Boise State University, Boise, Idaho, United States

Professional Preparation:

ORGANIZATION AND LOCATION	DEGREE (if applicable)	RECEIPT DATE	FIELD OF STUDY
University of Calgary, Calgary, Alberta, Canada	PHD	09/2016 - 07/2022	Electrical and Computer Engineering
University of Calgary, Calgary, Alberta, Canada	BS	09/2011 - 04/2016	Electrical and Computer Engineering

Appointments and Positions

2026 - present Assistant Professor, Boise State University, Boise, Idaho, United States
2024 - 2025 Research Associate, McMaster University, Hamilton, Ontario, Canada
2022 - 2025 Analog Circuit Engineer, NXP Semiconductors, Chandler, Arizona, United States
2016 - 2022 Graduate Researcher, University of Calgary, Calgary, Alberta, Canada

Products

Products Most Closely Related to the Proposed Project

1. Delshadpour S, Sheldon AW., inventors. NXP USA Inc., assignee. Passive equalizer. United States US12483449B2. 2025 November 25.
2. Sheldon A, Belostotski L. A Cryo-CMOS Low-Noise Amplifier With 2.3-to-8.5-K Noise Temperature at 20 K for Highly Integrated Radio-Astronomy Receivers. IEEE Microwave and Wireless Components Letters. 2022 November; 32(11):1319-1322. Available from: https://ieeexplore.ieee.org/document/9791109/ DOI: 10.1109/LMWC.2022.3178579

Other Significant Products, Whether or Not Related to the Proposed Project

1. Sheldon A, Belostotski L, Mani H, Groppi C, Warnick K. Cryogenic Noise-Parameter Measurements: Recent Research and a Fully Automated Measurement Application. IEEE Microwave Magazine. 2021; 22(8):52-64. Available from: https://ieeexplore.ieee.org/document/9475609/ DOI: 10.1109/MMM.2021.3078027
2. Elamien M, Sheldon A, Maundy B, Belostotski L, Elwakil A. Delay-Tunable Compact *RC*-Only All-Pass Filter. IEEE Microwave and Wireless Components Letters. 2021; 31(5):461-464. Available from: https://ieeexplore.ieee.org/document/9389535/ DOI: 10.1109/LMWC.2021.3069507

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3. Sheldon A, Belostotski L. Noise-Parameter Measurements of Very-Low-Noise Amplifiers at Ambient and Cryogenic Temperatures. IEEE Instrumentation & Measurement Magazine. 2021; 24(2):79-83. Available from: https://ieeexplore.ieee.org/document/9400953/ DOI: 10.1109/MIM.2021.9400953
4. Sheldon A, Belostotski L, Messier G, Madanayake A. Impact of Noise Bandwidth on Noise Figure. IEEE Transactions on Instrumentation and Measurement. 2019; 68(7):2662-2664. Available from: https://ieeexplore.ieee.org/document/8664192/ DOI: 10.1109/TIM.2019.2900145

Certification:

I certify that the information provided is current, accurate, and complete. This includes, but is not limited to, information related to current, pending, and other support (both foreign and domestic) as defined in 42 U.S.C. § 6605.

In accordance with Section 10632 of the CHIPS and Science Act of 2022 (42 U.S.C. § 19232), each individual identified as a senior/key person must certify that they are not a party to a malign foreign talent recruitment program.

Research Security Training Requirement for Federal Award Personnel: In accordance with Section 10634 of the CHIPS and Science Act of 2022 (42 U.S.C. § 19234), each individual identified as a senior/key person must certify that they have completed the requisite research security training that meets the requirements specified in Item 2 of Important Notice No. 149 within 12 months prior to proposal submission.

Certified by Sheldon, Alexander Wayne in SciENcv on 2026-02-23 12:05:59

APPENDIX C: SENIOR PERSONNEL

- **Alex Sheldon (PI), Boise State University**—Will use robust academic and industrial experience in designing high-speed analog integrated circuits to lead the project. Will guide students and coordinate all team member activity and communication and information sharing strategies while being attentive to project scope, budget, and schedule.
- **Doug Hackler, American Semiconductor**—As the chief executive officer of American Semiconductor in Boise, Mr. Hackler has committed to work with the Boise State research group to advance packaging capability towards the low-cost (in volume), and automatically aligned assembly process that would be required to economically manufacture the proposed NICs
- **Kjersti Martino, Inneos**—Dr. Martino at Inneos in Pleasanton, California who will provide the vertical-cavity surface-emitting lasers (VCSELs) used to drive the optical fiber. Inneos has agreed to provide product samples for the proposed prototype.

American Semiconductor
6987 W Targee St
Boise, ID 83709
208.336.2773

February 20, 2026

Alex Sheldon
Assistant Professor
Electrical & Computer Engineering
Boise State University

Letter of Support: Grant Application for "Design of a Low-Cost Optical Wavelength Division Multiplexing Transceiver in CMOS"

American Semiconductor fully supports Dr. Alex Sheldon's IGEM HERC proof-of-concept phase proposal titled "Design of a Low-Cost Optical Wavelength Division Multiplexing Transceiver in CMOS." If successful, we believe that this work will be a valuable contribution to the industry and could lead to a positive impact for Idaho economic growth.

As an Idaho-based company specializing in ultra-thin integrated-circuit packaging and advanced substrates we are uniquely positioned to package the integrated circuits and manufacture the substrates designed by Dr. Sheldon's research group with the VCSELs provided by Inneos.

As part of this project, American Semiconductor is committed to supporting Dr. Sheldon's research group in the design of the new substrate, based on our Nobleflex™ and Ultraflex™ technologies, and to enable the packaging of their integrated circuit with the VCSELs from Inneos. We are committed to collaborating with Dr. Sheldon's group in development of the test fixtures that are needed to enable the team to characterize and optimize the performance at the high frequencies required for successful completion of the project. We anticipate the project will include prototype manufacturing support for the 3-4 samples of the device needed for validation.

We believe this project will help to develop novel intellectual property in the state of Idaho which could be leveraged to bring a product to market. Assuming the project is successful, we would be able to continue to provide manufacturing capability for Boise State University or a future start-up company to ramp the new product to production.

Sincerely,

Doug Hackler
Chief Executive Officer
American Semiconductor

4255 Hopyard Road
Suite 105
Pleasanton, CA 94588

www.inneos.com

Phone: 925.226.0138
Fax: 925.226.0139

February 18, 2026

Alex Sheldon
Assistant Professor
Electrical & Computer Engineering
Boise State University

Letter of Support: Grant Application for "Design of a Low-Cost Optical Wavelength Division Multiplexing Transceiver in CMOS"

To Whom It May Concern:

I am writing on behalf of Inneos to express our support for Dr. Alex Sheldon's proposed research project titled "Design of a Low-Cost Optical Wavelength Division Multiplexing Transceiver in CMOS." We believe this work addresses an important challenge in optical interconnect technology and aligns closely with Inneos' mission to advance practical, high-performance optical solutions through thoughtful engineering and collaboration.

Inneos is a U.S.-based designer and manufacturer of vertical-cavity surface-emitting lasers (VCSELs), with particular expertise in wide-temperature-range and high-reliability devices for demanding environments. We have a strong interest in scalable, cost-effective optical architectures that can extend the benefits of wavelength division multiplexing to new applications and broader markets.

As part of this project, Inneos will support Dr. Sheldon's research by providing shortwave wavelength division multiplexing (SWDM) VCSEL devices for initial prototype development and testing. These devices will enable early validation of the CMOS-based transceiver architecture and allow the research team to evaluate key system-level parameters. We are particularly encouraged by the project's focus on low-cost implementation in standard CMOS processes, which has the potential to significantly reduce barriers to adoption for WDM-based optical links.

Inneos is pleased to support this effort and looks forward to the technical insights that will emerge from Dr. Sheldon's research. We believe this project will contribute valuable knowledge to the optical engineering community and help advance the state of integrated photonic systems.

Sincerely,

Kjersti Martino
Director of Product Management
Inneos